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14. ABSTRACT
The focus of the Center is to develop and demonstrate novel materials, both for device structures that advance the state-of-the-art in flexible electronics, as well as for environmentally-stable, hybrid, organic/inorganic semiconductors, leading to robust luminescent devices for flexible displays for the U.S. soldier. Performance of transparent and conducting oxides of indium tin oxide and F-doped ZnO films on plastics and their stability under mechanical deformation were investigated. Thin film transistors (TFTs) with gallium tin zinc oxide (GSZO)

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Report Title

Center of Excellence for Battlefield Capability Enhancements: Envronmentally Stable Flexible Displays

ABSTRACT

The focus of the Center is to develop and demonstrate novel materials, both for device structures that advance the state-of-the-art in flexible electronics, as well as for environmentally-stable, hybrid, organic/inorganic semiconductors, leading to robust luminescent devices for flexible displays for the U.S. soldier. Performance of transparent and conducting oxides of indium tin oxide and F-doped ZnO films on plastics and their stability under mechanical deformation were investigated. Thin film transistors (TFTs) with gallium tin zinc oxide (GSZO) channels, using the bottom gate configuration, were fabricated on thermally grown silicon dioxide on Si wafers. The best TFT electrical characteristics, with a threshold voltage of 4V and a drain current of 10-6A with an on/off current ratio as high as 106, have been obtained on RT deposited channel layers, annealed subsequently in air at 250 oC for 1 hr. on a 50 μm channel length and width. Inverted, hybrid organic light emitting diode structures that integrates inorganic and organic semiconductors layers were developed, with threshold voltage < 6V, efficiency > 2cd/A with operating lifetimes >500 hours without encapsulation. Preliminary results on monolayer molecular functionalization of inorganic semiconductors and charge injection from inorganic to organic semiconductors have been shown.

Enter List of papers submitted or published that acknowledge ARO support from the start of the project to the date of this printing. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

Received	Paper
2011/01/21 1: 8	A. Bowen, J. Li, J. Lewis, K. Sivaramakrishnan, T.L. Alford, S. Iyer. The properties of radio frequency sputtered transparent and conducting ZnO:F films on polyethylene naphthalate substrate, Thin Solid Films, (2010): . doi:
2009/11/11 1: 4	L.Wu, S. Iyer, J. Li, K. Gibson, J. Reppert, A. M. Rao, K. Matney, and J. Lewis. A study of low-temperature growth of III-V alloys for transparent layers, J Vac. Sci. Technol. B, 27(6), 2375 (2009), Journal of Vacuum Science Technology, (2009): . doi:

TOTAL: 2

Number of Papers published in peer-reviewed journals:

(b) Papers published in non-peer-reviewed journals (N/A for none)

Received	Paper

TOTAL:

Number of Papers published in non peer-reviewed journals:

(c) Presentations

1. Adam Bowen, “The Properties of RF Sputtered ZnO:F Thin Films Deposited on Polyethylene Naphthalate and Glass Substrates”, FlexTech Alliance 2011 Flexible Electronics and Displays Conference and Exhibition, February, 2011
2. Robert Alston, “Device Characteristics of Thin Film Transistors with Gallium Tin Zinc Oxide Channel Layers”, FlexTech Alliance 2011 Flexible Electronics and Displays Conference and Exhibition, February, 2011
3. Tanina Bradley, Robert Alston., J. Lewis, Garry Cunningham and Shanthi Iyer, “Device Characteristics of Thin Film Transistors with Gallium Tin Zinc Oxide Channel Layers”, Selected for student oral presentation at MRS/AVS/ASM North Carolina symposium, November 19th 2010, Raleigh, NC.
4. T. Bradley, R. Alston, S. Iyer, J. Lewis and G. Cunningham, “Amorphous Gallium Tin Zinc Oxide Films and TFT Performance for Flexible Electronic Implementation”, North Carolina Nanotechnology Commercialization Conference, March 31st-April 1st 2010, Koury Convention Center,Greensboro, NC, Awarded 1st place in Poster Presentation.

Number of Presentations: 1.00

Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Received	Paper

TOTAL:

Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Peer-Reviewed Conference Proceeding publications (other than abstracts):

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(d) Manuscripts

Received	Paper
2010/09/15 18 7	A. Bowen, J. Li, J. Lewis, K. Sivaramakrishnan, T.L. Alford, and S. Iyer. Adam Bowen et al.: "The Properties of Radio Frequency Sputtered Transparent and Conducting ZnO:F Films on Polyethylene Naphthalate Substrate", Provisionally accepted in Thin Solid Films, ( )
2010/03/16 15 5	A. Bowen, J. Li, J. Lewis, K. Sivaramakrishnan, T.L. Alford, and S. Iyer. The Properties of RF Sputtered Transparent and Conducting ZnO:F Films on Polyethylene Naphthalate Substrate-Submitted to Thin Solid Films, Thin Solid Films ( )
2008/10/06 16 3	L.Wu, S. Iyer, K. Gibson, and J. Lewis, K. Matney, J. Reppert, A. M. Rao, J. Li. A study of low-temperature growth of III-V alloys by molecular beam epitaxy for organic/inorganic hybrid devices -submitted to J. Appl. Phys.
	, ( )

TOTAL: **3**

Number of Manuscripts:

Books

Received	Paper

TOTAL:

Patents Submitted

Patents Awarded

Awards

Joint Faculty Appointment in Joint School of Nanoscience and Nanoengineering -2010
DoD National HBCU/MI Committee Member (2010) to assess HBCU's participation in their educational and research programs.

Graduate Students

NAME	PERCENT_SUPPORTED	Discipline
Robert Alston	0.25	
Jonathan Poe	0.35	
Shereen Farhana	0.50	
FTE Equivalent:	**1.10**	
Total Number:	**3**	

Names of Post Doctorates

NAME	PERCENT_SUPPORTED
Jia Li	0.40
Sudhakar Bharatan	0.40
FTE Equivalent:	**0.80**
Total Number:	**2**

Names of Faculty Supported

NAME	PERCENT_SUPPORTED	National Academy Member
Shanthi Iyer	0.00	
FTE Equivalent:	**0.00**	
Total Number:	**1**	

Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED	Discipline
Sinelik Berhane	0.00	Electrical and Computer Engineering
Jazmin Clark-Harris	0.00	Electrical and Computer Engineering
FTE Equivalent:	**0.00**	
Total Number:	**2**	

Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period:	2.00
The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:.....	2.00
The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:.....	0.00
Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):	0.00
Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering:	0.00
The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense	0.00
The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields:	0.00

Names of Personnel receiving masters degrees

NAME
Robert Alston
Total Number: 1

Names of personnel receiving PHDs

NAME

Total Number:

Names of other research staff

NAME PERCENT SUPPORTED

FTE Equivalent:

Total Number:

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Center of Excellence for Battlefield Capabilities Enhancement: Environmentally Stable Flexible Displays

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Program Manager: Michael Gerhold

Shanthi Iyer, Principal Investigator

Department of Electrical and Computer Engineering
North Carolina A&T State University
Greensboro NC 27411

Jay Lewis, Co-Principal Investigator

RTI International
3040 East Cornwallis Road
Post Office Box 12194
Research Triangle Park, NC 27709-2194

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APPENDIX

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B. L. Wu et al., *J. Vac. Sci. Tech. B,* 27, 2375-2383(2009).
C. A. Bowen et al., *Thin Solid Films*, 519, 1809 (2010).

Center for Excellence for Battlefield Capability Enhancements: Environmentally Stable Flexible Displays
Technical Description
Grant No: W911NF-04-2-0051

This is the final technical report describing the research activities of the Battlefield Center of Excellence Center. The focus of the Center was to develop and demonstrate novel materials, both for device structures that advance the state-of-the-art in flexible electronics, as well as for environmentally stable, high-performance, hybrid organic/inorganic semiconductor, robust luminescent devices for flexible displays for the U.S. soldier.

There were two major research components to the Center. The first component constituted the investigation of (a) the novel transparent and conducting semiconductor material systems for organic light emitting diodes (OLEDs) and thin film transistor electrodes, (b) transparent amorphous oxide thin film transistors (TAO-TFTs) for flexible electronics and (c) the stability of transparent and conducting oxide (TCO) materials and devices under optical excitation, electrical bias and mechanical deformation. This component encompassed a highly collaborative effort of five institutions: NCA&TSU (**Iyer**'s group) as lead, RTI (**Jay Lewis** and **Garry Cunningham**), U.S. Army Flexible Display Center (FDC)/Arizona State University (**Terry Alford** and his student **Sivaramakrishnan**), and Army Research Laboratory (**Eric Forsythe**).

The second component of the research effort pertained to hybrid device technology. The primary goals of this effort were improved performance and stability, compared to conventional OLEDs, and ultimately transitioning the technology to field demonstrators. This work was primarily being carried out by RTI, International with NCA&TSU in collaboration.

Student training, educational component and technology transition from RTI International to NCA&TSU were the other major goal of this collaborative research.

The report has been delineated into two major sections. The first one details the first component research outcome, student participation and infrastructure developed at/transitioned from RTI to NCA&TSU campus and the other section refers to the second research component carried out primarily at RTI, International. In both the sections, a brief list of summary of accomplishments achieved every year followed by technical progress made each year are presented.

1. Novel Transparent and Conducting Semiconductor Material Systems, TAO-TFTs and their Stability

1.1 Summary of Accomplishments

Year 1

- Preliminary results on the low temperature growth of various III-V alloys namely, GaAs, GaAlAs and GaAlAsN on non-crystalline substrates by molecular beam epitaxial (MBE) technique for wide band gap component of the hybrid LED device were shown to be very promising.
- Student training at RTI, international in implementing self-assembled monolayers on different substrates.

Year 2

- A systematic and detailed work on the low temperature (<300ºC) growth of III-V layers by molecular beam epitaxial (MBE) technique by studying the effect of each component in the AlGaAsN system on surface morphology, structural and optical properties on different unconventional substrates were carried out.
- Successful growth of transparent AlGaAsN layers on ITO/glass exhibiting transmission better than 90% in visible region with surface roughness of 10 nm and less with fairly good adhesion was demonstrated.
- Kellen Gibson-M.S. Thesis completed. Kenneth Lee- undergraduate student trained on the mechanical testing of the flexible component at RTI International and summer interned at FDC, AZ.
- Graduate course on flexible display was being developed to be offered at NCA&TSU during the year 3 of the project.

Year 3

- Detailed Raman characterization was carried out to get a more insight into the bonding in the wide band gap GaAlAsN material system grown at low temperatures. The good quality GaAlAsN layers exhibit preferential AlN bonding at 465 cm^{-1} in the Raman spectra.
- Attempts to doping of the MBE grown III-V-N layers were not successful. Limited success was achieved on the charge injection into the III-V-N layers using Au contacts.
- Collaborative (RTI, ASU and NCA&T) study to correlate the deposition process parameters for ITO films on PEN substrates with the electrical, chemical and mechanical properties was completed and submitted to Thin Solid Films for publication.
- Successful mechanical test capability was established at NC A&TSU.
- Successful self assembled monolayers (SAM) coverage work was transitioned to NCA&TSU.

- A course on “Display Technology” (ELEN 685) was offered during Spring 07, semester to the senior undergraduates and graduate students of Electrical and Computer Engineering at NCA&TSU.
- As a seed project GaAs nanowires were successfully synthesized on Si substrates.

Year 4

- The effects of growth process parameters and the substrates on the surface morphology, structural and optical properties of the MBE grown GaAlAsN layers, using a variety of characterization techniques, namely x-ray diffraction (XRD), atomic force microscopy (AFM), Raman, and transmission spectra, were analyzed. To the best of our knowledge, these are the first low temperature studies of III-V-N semiconductors on polycrystalline and glass substrates by any technique. This work was submitted to J. Vac. Sci. Tech. B.
- Sputter deposition system was installed at NCA&TSU. Collaborative (RTI, ASU, ARL and NCA&T) study to correlate the sputter deposition process parameters for ZnO films on PEN substrates with the structural, electrical, optical and mechanical properties was completed and the manuscript was being in preparation for submission to a suitable journal.
- Mechanical evaluation of the above ZnO films were carried out using the in-house mechanical test capabilities designed at NC A&TSU.

Year 5

- The work on the III-V MBE grown alloys which began at the inception of this grant was brought to completion during this funding period by carrying out extensive absorption studies and correlating with other properties of the layers. The work was accepted for publication in J. Vac. Sci. Tech. B.
- Systematic study of correlating the sputter deposition process parameters of F-doped ZnO films on PEN substrates to the structural, electrical, optical, and mechanical properties was continued.
- ZnO:F films of thickness 100 nm deposited on PEN substrate at room temperature with post deposition annealing in either Ar or 7% H_2/Ar ambients the annealed films deposited on PEN substrate reveal high transmission of 80%, $N = 6.7\text{x}10^{19}/\text{cm}^3$, $\mu = 9.5\ \text{cm}^2/\text{V-s}$ and $\rho = 1.3\text{x}10^{-2}\ \Omega\text{-cm}$. This work on ZnO;F films was brought to completion and the work was submitted to Thin Solid Films for publication.
- A device stability system was set up that would visually record the degradation of the OLED devices over time under bias conditions as well as during bend testing.
- Thin film transistor with bottom gate configuration and a gallium tin zinc oxide (GSZO) channel was fabricated for the first time.

Year 6

- All the processing and fabrication of the TFT were transitioned to NCA&TSU. TFTs were all fabricated in-house.
- Detailed investigation of TFT with GSZO channel on Si was carried out as a function of oxygen partial pressure during the sputtering and substrate temperature.

- Optimal characteristics for a 50 µm x50 µm transistors achieved in the depletion mode exhibited an I_D of $2x10^{-6}$ A, V_T of -1 V and $I_{on/off}$ of $4x10^6$, while in the enhancement mode exhibited an I_D of 10^{-6}A, with V_T of 4 V and $I_{on/off}$ of 10^6.

1.2. Summary of Technical progress

Year 1

i. Low Temperature Growth of III-V Alloys by MBE

The goal of the year 1 was to examine different III-V inorganic alloys that are compatible for low temperature growth and exhibiting wide band gap for optical transparency in the visible region. As the pyrometer commonly used during the MBE growth is not operable below 400 °C, calibration procedures for the measurement of the substrate temperature at these lower temperatures were established (see Progress Report 1[1] and subsequent publication[2]).

As there was no data available in the literature on the low temperature growth of these alloys as well as on unconventional substrates namely indium tin oxide coated Si (Si-ITO) and quartz glass, a preliminary study of the growth of the binary GaAs was followed by alloying with Al and N separately to find the feasibility of the growth of these layers at low temperature. Finally quaternary arsenide-nitride alloys of GaAlAsN were also demonstrated. Different techniques namely x-ray diffraction, atomic force microscopy and reflectance measurements were used for the characterization of these layers.

ii. Student Participation and Education Component

Kellen Gibson, a graduate student was trained on the MBE system and characterization of the III-V layers as a part of his M. S. thesis. He was also being trained at RTI International, in implementing self assembled monolayers on different substrates.

Year 2

i. Low Temperature Growth of III-V Alloys by MBE

Though successful growths of GaAs, GaAlAs and GaAlAsN on unconventional substrates such as glass and indium tin-oxide (ITO) coated glass below 300 °C by molecular beam Epitaxy (MBE) were demonstrated the 1st year, the band gap was in the near infrared region and Al and N had no influence on the band gap. Hence a systematic and detailed study was carried out at by optimizing first the low temperature growth parameters for the GaAs growth followed by AlAs, which represented the other extreme composition in terms of roughness and the transmission properties. Then, the effect of each additional constituent element Al and N to GaAs on the surface morphology, structure and optical properties of the layers, was studied in a systematic way. Finally, the growth parameters were explored such as N flux, plasma power on the final alloy composition of GaAlAsN to fine tune the growth condition for realizing the high band gap material with good surface morphology, as displayed in Figure Y2.1.

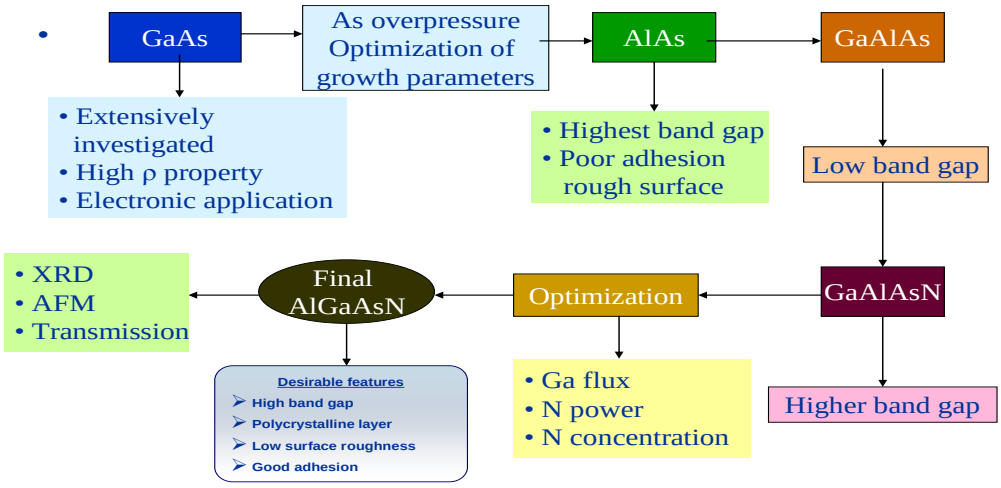


Figure.Y2.1. Schematic of the approach adopted and summarized results.

Finally, inverted gate thin film transistor (TFT) structures using the GaAlAsN channel layers were fabricated on Si substrate but were not functional.

ii. Student Participation and Education Component

Kellen Gibson, successfully defended M.S. Thesis entitled "A Preliminary Investigation of Low Temperature Growth of III-V Compound Semiconductor Materials and Growth of Self-Assembled Monolayer Materials for Hybrid Organic Light Emitting Diode Applications". **Jay Lewis** from RTI, International served on his thesis committee.

Kenneth Lee, an undergraduate senior, carried out mechanical testing of the transparent and conducting indium tin oxide (ITO) films on the polyethylene napthalate (PEN) substrates at RTI, International. The films were provided by Terry Alford from ASU/FDC. He also visited Flexible Display Center at Arizona State University during the summer and worked under the guidance of **Jann Kaminski** and **Sameer Venugopal.** He successfully completed a couple of small projects on programming using labview program and pixel circuit testing. An informal project report [3] was sent to the technical monitor. This student summer internship opportunity arranged in a short notice came to fruition due to the coordination of **Vallen Emery** and **Eric Forsythe** from ARL, **John Zavada** from ARO, **Gregory Raupp** from the Flexible Display Center @ Arizona and numerous staff from ARO and NCA&TSU.

The work on mechanical testing was transferred from Kenneth Lee to another undergraduate student **Richard Berryman. Tanina Bradley** (minority female student), a fresh Ph.D. candidate, continued the work of **Kellen Gibson** on SAM.

In addition four senior undergraduate students **Cynthia Prince, Chanavia Johnson, Kineta Lewis,** and **Stan Potoczny** began design and construction of the bending fixture modeled after collapsing radius bend testing system at RTI, International. This was made as a part of the senior design undergraduate project, in partial fulfillment of the requirements for the

undergraduate Electrical Engineering degree program. This project began under the supervision of **Greg Gilmore**, from the Department of Electrical and Computer Engineering, NCA&TSU.

A graduate course on "Display Technology" was being developed by **Shanthi Iyer** and **Jay Lewis,** scheduled to be offered during the Spring 2007 at NCA&TSU.

iii. Infrastructure Development

Stan Potoczny (an undergraduate student), who is also a part of the above senior design project, developed the quote for the scanning tunneling microscope to upgrade the MBE system that would provide a powerful in-situ diagnostic tool for the growth mechanism on an atomic scale to be integrated with the MBE system as well as a quote on glove box for the SAM project.

Design and construction of bend testing fixture as described in the above section also began this 2nd year of the grant period.

Year 3

i. Low Temperature GaAlAsN MBE Growth

Detailed Raman analysis was carried out on MBE grown unoptimized GaAlAsN layers as well as optimized AlGaAsN grown on glass substrates. Unoptimized GaAlAsN layers exhibited very few peaks which were broad indicative of deteriorating quality of the layers, while the optimized layer exhibited a sharp AlN TO peak which was also confirmed by examining the AlAsN reference layer grown on glass. The details of these are presented in our third report[4] as well as our publication[2].

ii. Doping and Charge Injection in III-V Layers

The presence of large defects renders these layers highly resistive and hence doping of these layers poses a great challenge. Different n-type dopants were attempted which include Si, SnTe and Ga_2Te_3. We believe Ga_2Te_3 is a promising dopant due its high vapor pressure at the growth temperature (250^{o}C) and as a result operating Ga_2Te_3 cell temperature is quite low around 475^{o}C. Based on few runs we have not observed any change in resistivity with this as the dopant and on the contrary resulted in poorer transmission. This calls for investigation of novel captive sources.

The next step was to investigate the charge injection behavior on the III_V semiconductors grown. These were evaluated using the MIS configuration as shown in Figure Y3.1 (a) where one half of the layer was coated with Al contacts and the other half of the layers were coated with Au. Au contact was found to be more successful than Al contact. The I-V characteristics obtained using the Au contacts are illustrated in Figure Y3.1 (b). Nonlinear I-V behavior is indicative of space charge limited injection. The structure was more prone to shorting due to the rough surface morphology of the layers.

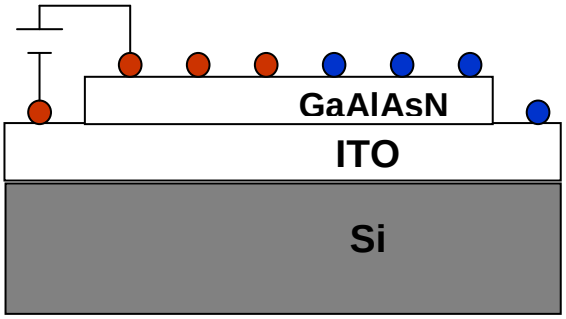


Figure Y3.1 (a). Schematic of the MIS structure

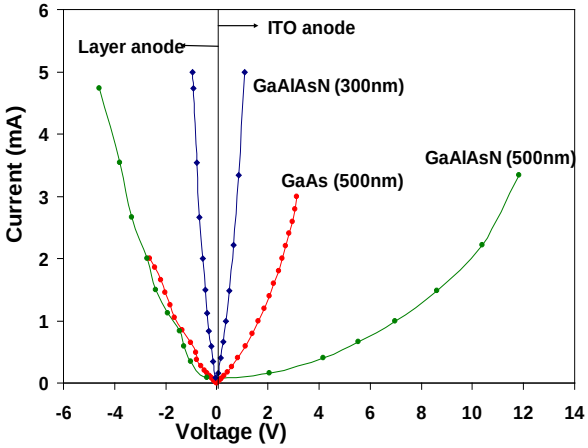


Figure Y3.1 (b). I-V data for GaAlAsN and GaAsN MIS structures for different thickness with Au top contact.

The pursuit to improve upon the above work was interrupted due to more promising results obtained in the charge injection from ZnO layers directly into Alq3 as discussed later in section 2. Hence our efforts were currently directed towards acquisition and setting up the sputtering unit at NCA&TSU for the deposition of ZnO doped layers.

iii. Molecular Functionalization of Inorganic Semiconductors

Glove box was installed at NCA&TSU and all the self assembled monolayer coverage procedures were transitioned from RTI International to NCA&TSU. The details of the work are described under the section 2 Year 3, which were carried out by Tanina Bradley.

iv. Deposition of ZnO:Al at ARL

As the charge injection from transparent conducting oxide layers have found to be more promising (see Year2 of Section 2), the efforts were directed towards setting up a sputtering system at NCA&TSU. **Stanley Potoczny**, an undergraduate senior was sent to **Army Research Laboratory (ARL) @ Delphi** as a summer intern to get training in the operation of the sputtering unit. He worked in **Eric Forsythe's** group on the deposition of ZnO:Al films on glass substrates. Different RF sputtering units which existed in the ARL laboratory were used, which included a Denton Sputtering unit and a custom made multi- tool vacuum units equipped with RF magnetron. ZnO/Al_2O_3 doped with 6 wt% Al_2O_3 was used as the target. As the partial pressure of the oxygen could not be accurately calibrated in the system the only variables that were used for optimizing the film properties were the deposition time and source to target distance (D(s-t)). Transmission characteristics did not exhibit any change with source to target distance though it decreased with increasing deposition time due to the larger thickness as expected as shown in the Figure Y3.2. Some of these substrates were used for the deposition of self assembled monolayer as discussed later in Year 3 of section 2.

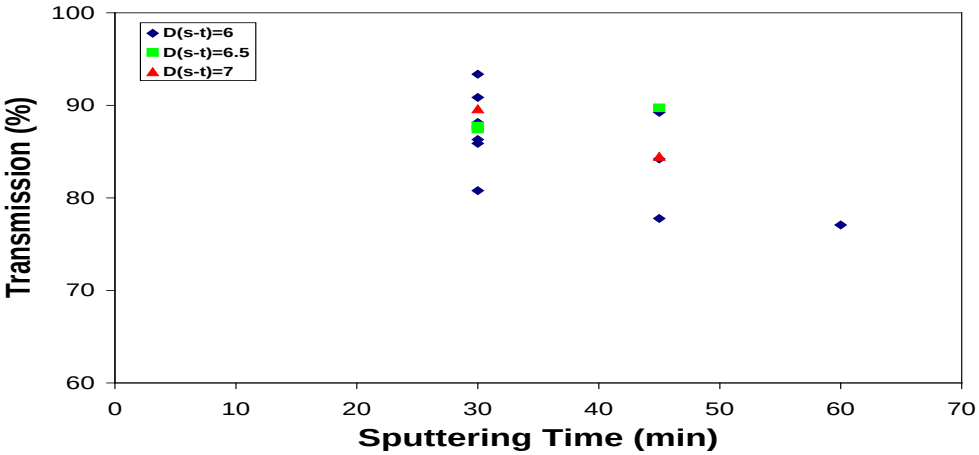


Figure Y3.2. Transmission of the layers as a function of sputtering duration for different source to target distances (D(s-t)).

v. Seed Project: GaAs Nanowire (NW) Growth

Semiconductor nanowires (NWs) are currently revolutionizing the electronics and optoelectronic research fields due to the synthesis of these structures virtually free of defects and isolation of the high temperature synthesis from assembling and processing of these NWs for device fabrication. This allows fabrication of devices entirely at room temperature on any substrates. These unique features lend themselves for entirely a new class of high performance NW-thin film transistor (TFT) on plastic substrates where all the processes involved are room temperature. Extensive work has been carried out on Si NW-TFT's which can be easily adapted to III-V NW TFT's. The latter in principle should show much better performance than Si counterparts due to the inherent higher carrier mobility exhibited by III-V semiconductors. Also the favorable optical properties exhibited by these semiconductors would allow realization of multifunctional devices on flexible substrates that have not been hitherto envisaged.

Hence, the synthesis and assembling of nanoscale materials are the two important aspects towards understanding the fundamental properties of the nanostructure materials and enabling nanotechnology. Numerous techniques have been developed for the synthesis of NW striving for control over the key structural, chemical and physical properties. Synthesis induced by metal catalysis has been the most commonly used technique for the NW growths.

A few MBE growth runs of GaAs nanowires using 4-10 Å thick Au films prepared by thermal evaporation on (001) Si are shown in Figure.Y3.3(a) The SEM photograph of GaAs wire deposited at 530°C revealed long and tapered wires. Room temperature photoluminescence (RT PL) measurements on a single NW exhibited a 5 nm blue shift in comparison to the bulk GaAs and the corresponding Raman spectra displayed LO - phonon mode suppression. These spectral signatures are clear evidences of quantum confinement. X-ray diffraction of these wires exhibited a stronger GaAs <111> diffraction peak in comparison to the <220> and <311> peaks as shown in Figure Y3.4.

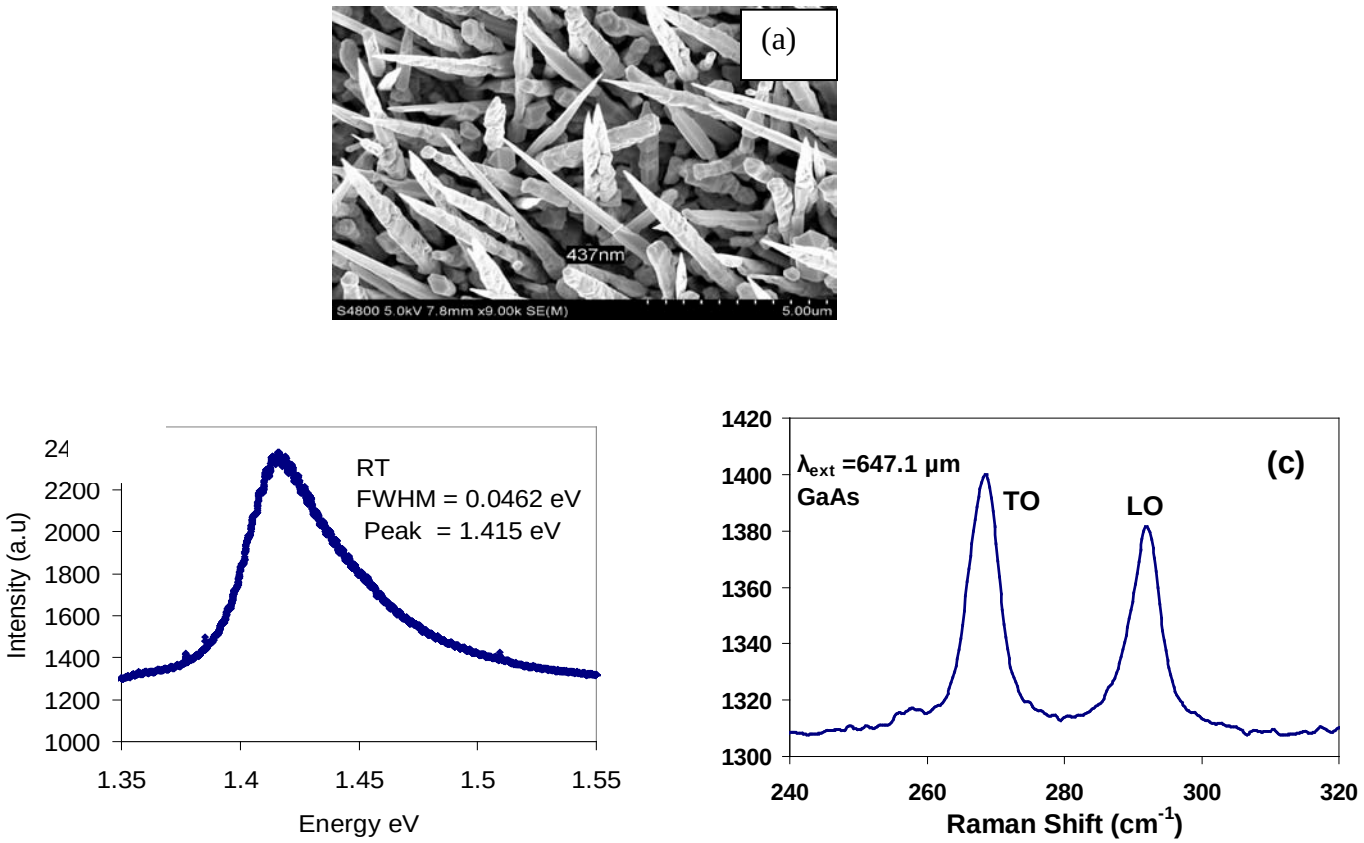


Figure Y3.3. (a) SEM photograph of GaAs NWs, (b) RT PL of single NW and (c) Raman spectra

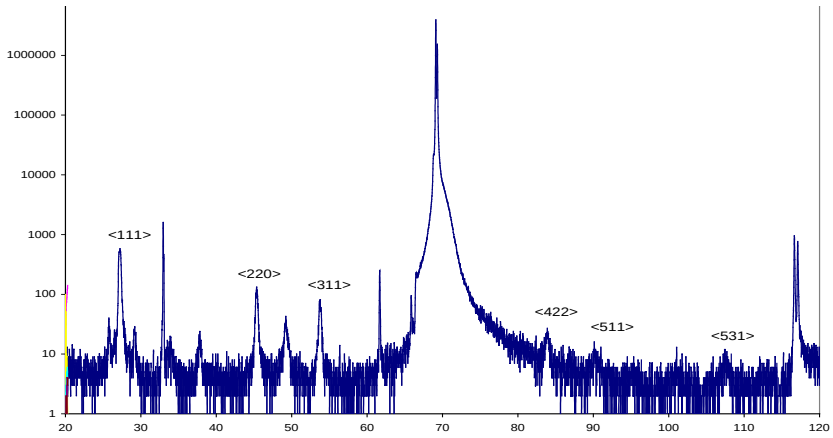


Figure Y3.4. X-ray diffraction of the NWs with <111>, <220>, <311> diffraction

It is to be noted that these were very preliminary results and the Au film was deposited ex-situ by **Rao's** group at Clemson University, while the MBE growth was carried out at a later time at

NCA&TSU. This preliminary success clearly indicated considerable potential for improving the quality and tailoring the properties of the NWs grown.

vi. Student Participation and Educational Component

Four senior undergraduate students **Cynthia Prince, Chanavia Johnson, Kineta Lewis,** and **Stan** Potoczny who began the design of the collapsing radius bending fixture during the year 2 as a part of their senior undergraduate design project under the supervision of **Dr. Greg Gilmore** completed the project in the 3 year of the grant. The project was implemented in two phase. The first phase of the program entailed the design of the translation system, selection and procurement of appropriate motors, followed by the design and demonstration of a motor control system. The second phase of the project, during the spring 2007, involved integration of the translation system with the appropriate sample fixtures. Data logging as shown in Figure Y3.5, motion control software, and analysis of the failure of conductive layers on a flexible substrate were demonstrated. The students also improvised on the existing bending apparatus in particular, to improve upon shortcomings of the existing system at RTI, International, such as preventing kinks when the film is brought back to its original position after the bend testing. The bend testing system so constructed was very user friendly.

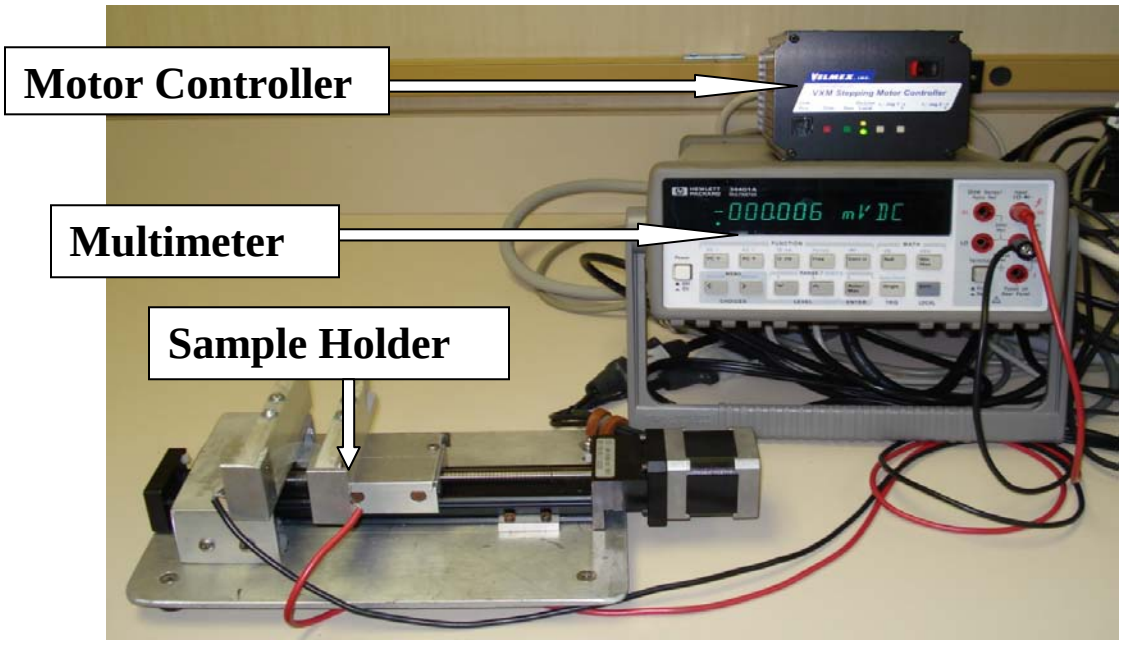


Figure Y3.5. Bend test system set up

A typical bend testing data that has been obtained on the system using PEN substrate is shown in Figure Y3.6. .This simple in-built bend testing system has become the work horse for testing the films grown on PEN substrates.

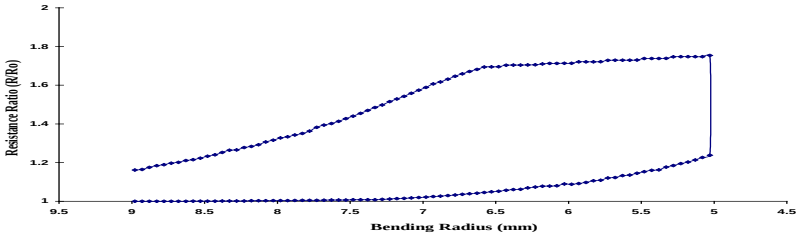


Figure Y3.6 Resistance Vs the bending radius test data

Stan Potoczny, an undergraduate, participant in the above senior design project graduated during this grant period. He summer (2007) interned at ARL in Adelphi, Maryland under the direct supervision of **Eric Forsythe**. He was trained in the operation of the sputtering unit and deposited successfully ZnO:Al doped layers as detailed above in section 4.

The work on SAM which was originally carried out by **Kellen Gibson** at RTI and NCA&TSU was taken over by **Tanina Bradley**, a Ph.D. candidate (afro-American female student) and her work has been described in RTI report section Y2.

Finally a course on "Display Technology" developed by **Shanthi Iyer** and **Jay Lewis** during the year 2 of the grant period was successfully offered during this period to the graduating seniors and graduate students (Figure Y3.7) during the spring semester at NCA&TSU. The course (detailed course content is provided in Appendix A) provided the basic concepts on the fundamentals of light and color as the basis for understanding different display technologies at an introductory level. Fundamental aspects of different types of optical signal generation were discussed. A review of common display technologies, typical applications of each, and some of the more interesting emerging technologies now on the horizon were also presented. Selected standards within the display industry were discussed in terms of the basic requirements and applications of each standard.


Figure Y3.7. Graduate and undergraduate students with Jay Lewis during the field trip for the "Display Technology" course

vii. Infrastructure Development

During this grant period a variable temperature ultra high vacuum scanning tunneling microscope from Omicron Nanotechnology was purchased from this funding. This is a custom bolt on extension to the existing MBE system consisting of chamber with an additional ports for buffer chamber, transfer devices, sample transfer viewing. It comes with a modular control system for scan generation, regulation and data acquisition. STM will be a powerful in-situ tool to study the morphology of the grown layers, the roughness, island shapes- their diameters and interspacing, surface reconstruction domains and pits-their relative coverage. They can also be used to determine the surface states and relative changes in the band bending at the interface, an importance for the low temperature deposition material system. A custom made stainless steel glove box from M. Braun for the SAM project was purchased and installed as shown in the Figure Y3.8 below and all the SAM coverage was transitioned to NCA&TSU.

Figure Y3.8 Stan Potoczny using the glove box

Stan Potoczny used his summer internship experience on sputter deposition techniques very fruitfully in identifying basic requirements for a sputter deposition system to be purchased at NCA&TSU. He developed the quote for the sputtering unit and a refurbished system Edwards ESM 100 sputter deposition machine that met all of the requirements for a system and also was within the budget, was ordered during this grant period.

Year 4

i. LT MBE Growth of Transparent III-V Materials

A systematic and detailed work on the low temperature (<300ºC) growth of numerous III-V layers namely GaAs, GaAlAs(N), and AlAs(N) by molecular beam epitaxial (MBE) technique during the last few years were used to arrive at an optimized composition for wideband gap applications with good surface morphology on different unconventional substrates. This resulted in successful growth of transparent AlGaAsN layers on ITO/glass exhibiting transmission better than 90% in visible region with surface roughness of 10 nm and less with fairly good adhesion. The effects of

growth process parameters and the substrates on the surface morphology, structural, and optical properties of the layers using variety of characterization techniques namely x-ray diffraction (XRD), atomic force microscopy (AFM), Raman, and transmission spectra were studied and this work was submitted to J. Vac. Sci. Tech. B. To the best of our knowledge, these were the first low temperature studies of III-V semiconductors on polycrystalline and glass substrates by any technique.

ii. ZnO Deposition by RF Sputtering

The other low temperature transparent and conducting material that was investigated during this grant period was from the family of transparent and conducting oxide materials. In the Year 3 indium tin oxide (ITO) films were deposited on PEN substrates. [See the section 2 Year 2 and refs. 4-6] In the Year 4 ZnO films were examined as these provide a much cheaper alternative compared to the increasing cost of in based material systems. Further, it also allows lower deposition temperatures and is more stable in activated hydrogen environments than other TCOs. Hence it is compatible with the deposition on flexible polymer substrates.

Though there have been reports in the literature on the electrical, optical, and mechanical properties of ITO grown on polymer substrates[5-7], no similar work has been reported on ZnO films. In this work we investigated F doped ZnO films deposited at room temperature with subsequent annealing not exceeding 150 ˚C in order to be compatible with polymer temperature thresholds. F was chosen as F doped tin oxide has been reported[8] to lower the work function, one of the desirable characteristic that is being sought in these films for using them as an electrode material. The effects of annealing in different ambients and thickness of the films on the surface morphology, structural, optical, electrical properties and mechanical robustness of the films were the subject of study. This has been detailed in report[9] and also later published in thin solid films[10] and attached in the Appendix B.

iii. Infrastructure Development

(a)RF Sputtering Unit @ NCA&TSU

The Edwards ESM 100 Deposition System shown below in Figure Y4.1. was delivered in November 2007. The system consists of two 4**”** RF magnetron cathodes, and one heat station for in-situ annealing. The two 4” RF magnetron cathodes are powered by one Edwards Plasma Products RF-10, 1KW RF generator and automatic matching network for magnetron sputtering. Each cathode has its own manually operated shutter. The system is equipped with a Varian automatic valve sequencer for automatic pump down.

Upon acquisition of the system there were many requirements such as plumbing for water circulation, compressed air, electricity, drain, exhaust, necessary for installation so that the system may be made operational. Further, the system was also modified for an additional mass flow controller to process more than one gas and one heat station to carry out annealing in different ambients inside the chamber.

The stainless steel deposition chamber is 12 inches in diameter equipped with one two inch view port. With a counter balanced lid opening at the top of the chamber it is equipped for a sputter up configuration. The substrate holder is attached to the lid with a rotation speed of 24

rpm. The lid is configured with a 500 watt RF generator and automatic matching network for substrate biasing and substrate etching.

The system is equipped with an Edwards roughing pump and a CTI CryoTorr 8 cryopump. The system operating pressure is controlled by a throttle valve. Pressure is read from two pirani gauges and one terranova ion convectron vacuum gauge.

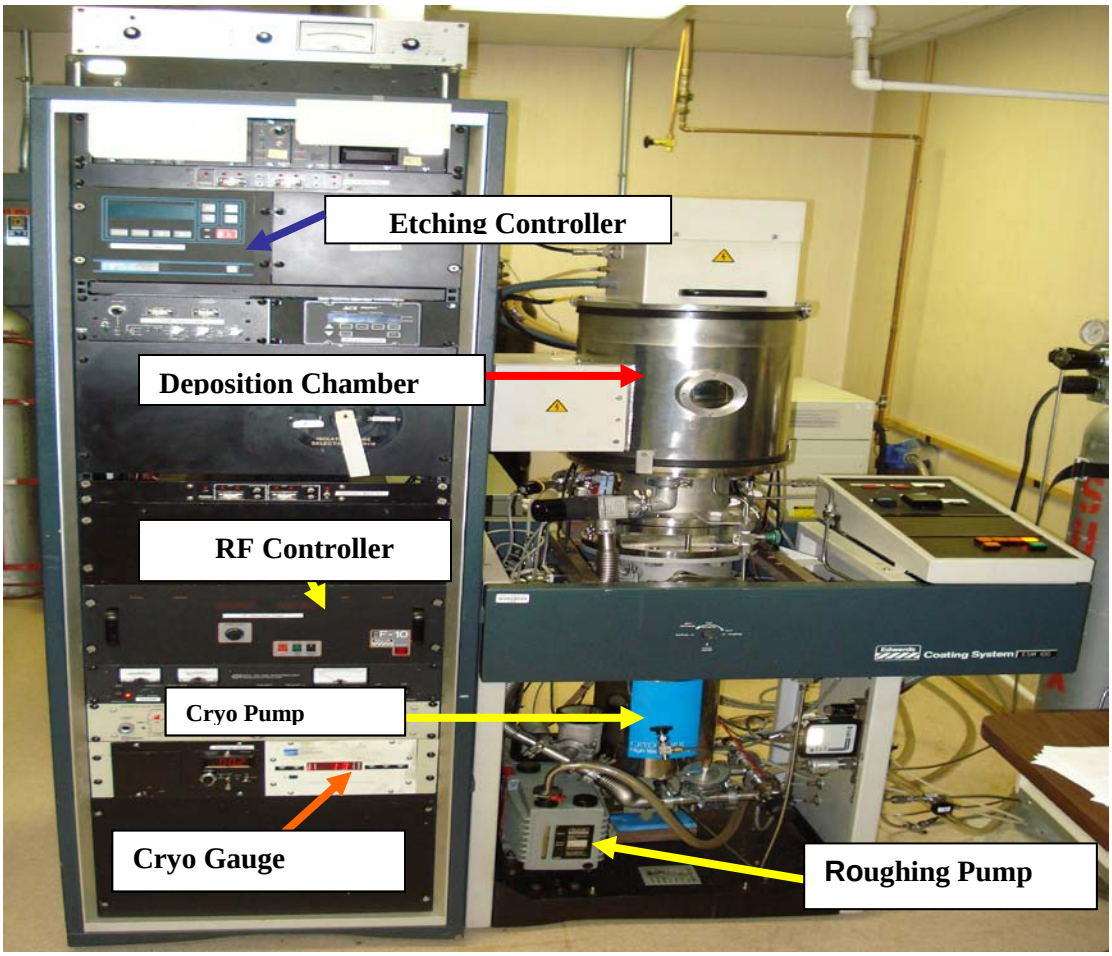


Figure Y4.1. : Edwards ESM sputter deposition System

One or more gasses can be precisely metered into the system using the two mass flow controllers. The system was originally outfitted with one MFC, however a second one was later added due to the need to introduce oxygen into the system. One MFC has been calibrated for the Ar process gas and the other is being used for oxygen or another specified gas as needed.

The in-situ heater was fabricated *in-house* from the existing Watlow heater controls and a new Kapton four inch heater pad. The heater is capable of reaching a max continuous temperature of 392˚ F or 200˚ C. Heating a sample is carried out by placing the sample onto the

pad, resuming normal pump down to desired vacuum and setting the heater controls to desired operating temperature. ZnO target with 2 wt. % ZnF_2 was installed for doping the layers with F.

iv. Student Participation and Education Component

The acquisition of the sputtering unit as well as installation and carrying out the research project on ZnO:F films have been carried out by **Adam Bowen** and **Stanley Potoczny** in fulfillment of the **Masters of Science thesis** requirements. Both students had a broad background in electrical and mechanical systems. Having such a technical background had complimented as well as accelerated the students in their ability to undertake this project and bring it to fruition within a very short span of 3-4 months.

Year 5

i. Transparent and Conducting Oxides for Contacts and Electrodes

(a) III-V-N Transparent Layers Grown by Molecular Beam Epitaxy (MBE) at Low Temperature on Glass

A systematic and detailed study on the layer property-composition relationship of the MBE grown III-V alloys at low substrates temperatures (< 200 ºC) on unconventional substrates, which began at the inception of this grant, was completed successfully during this funding period. Based on the review received from J. Vac. Sci. Tech. B extensive absorption edge studies of all the low temperature III-V MBE grown alloys were carried out and the revised version of the manuscript was accepted in the J. Vac. Sci. Tech B for publication[2], also attached in Appendix C.

(b) F-doped ZnO Films

The properties of ZnO: F films by RF sputtering on PEN substrates have been correlated to the thickness of the films and annealing ambient. Annealing in 7% H_2/Ar resulted in substantial grain growth and increased surface roughness, but had a significant effect on optical or electrical properties only for films thinner than 100 nm. The films deposited at room temperature and annealed in either Ar or 7% H_2/Ar ambients exhibited carrier concentrations between $2x10^{18}/cm^3$ and $9.5x10^{19}/cm^3$, mobility between 3 and 11 cm^2/V-s, and resistivity between 10^{-1} and 10^{-2} Ω-cm. At a thickness of 100 nm the annealed films deposited on PEN substrate reveal high transmission of 80%, $N = 6.7x10^{19}/cm^3$, μ = 9.5 cm^2/V-s and $\rho = 1.3x10^{-2}$ Ω-cm. The electrical transport properties were explained using the ionized impurity and lattice scattering mechanisms, and were identified as predominantly due to O vacancy scattering. Mechanical test capabilities for bend testing developed in year 3 by undergraduate students at NCA&TSU was extensively used, during this funding period, to test ZnO:F films to evaluate the mechanical integrity of the layers after they were bent. The bending radius used as a measure of the mechanical flexibility of the films was found to be around 13 mm for a 200 μm thick PEN substrate. Both annealing and thickness of the films determine the critical stress beyond which the failure of the film occurs, which in turn influences the critical radius of bending.

RBS studies were carried out by **Terry Alford's** group from ASU. This work was a result of a very collaborative work from RTI, ASU, ARL with NCA&TSU as a lead. The manuscript was submitted to thin solid films[10] for publication and attached in Appendix D. This work resulted in two M.S.E.E. theses[11,12].

ii. Transparent Amorphous Oxide Semiconductor TFTs

RF sputtered films of gallium tin zinc oxide (GSZO) has been the main focus of this funding period. These were investigated for TFT applications. Table Y5.1 lists deposition parameters of the RF sputtered films prepared from a 4" $ZnO/SnO_2/Ga_2O_3$, 88/7/5 wt% target. The oxygen processing pressure was varied during the deposition; this in turn varied the thickness of each sample. Glass samples were etched in argon plasma for 2 minutes with an etch power of 10 watts. They were pre-sputtered for 10 minutes with an oxygen gas flow of 5 sccm and argon gas flow of 100 sccm. The sputtering background base pressure was $6x10^{-6}$ Torr, with a process pressure of 5 mTorr. The deposition time was 35 minutes. Ellipsometry was used for thickness measurements. Surface roughness of these films on glass was typically around 5.7 nm RMS on a 5x5 µm atomic force microscope (AFM) image.

Annealing of the films in vacuum was carried out at different temperatures and durations to decrease the resistivity of the films, which was greater than Ω -cm on as-deposited films. Figure Y5.1 displays the variation of the resistivity with temperature and duration for films deposited on glass and PEN substrates. The resistivity of the films was found to depend on the type of the substrate, annealing temperature and duration. Higher temperature and duration yielded lower resistivity. The layers annealed on glass exhibited higher resistivity. The resistivity on the glass at 170 °C, annealed for as long as 8 hr in duration, was significantly higher than Ω -cm.

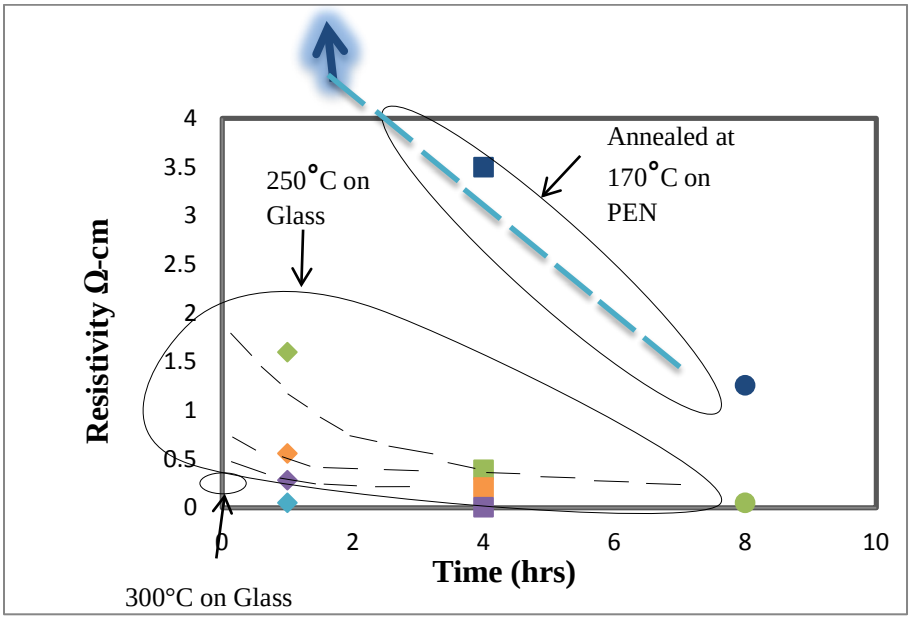


Figure Y5.1. Variation of GSZO film resistivity on glass and PEN substrates with annealing duration at different temperatures. Each of the color represents sample from different growth runs.

As there is a significant reduction in the resistivity for 4 hr annealing at the lower temperature end of 250 °C, all the samples listed in Table Y5.I underwent annealing at this temperature and duration. The highest mobility achieved was 12 cm^2/ V-sec, with a carrier concentration of $1.7x10^{16}$ cm^{-3} as measured by the Hall technique.

Table Y5.1. GSZO deposition parameters and electrical parameters of the films after annealing in vacuum for 4 hr.

Sample	Thickness (nm)	Ar Gas Flow/O_2 Gas Flow (sccm)	RF Dep Power (watts)	Resistivity (Ω-cm)	Mobility (cm^2/V-sec)	Carrier Concentration (cm^{-3})
60	193	100/0	120	0.3	3.4	$6.1x10^{18}$
61	82	100/0	75	0.9	3.8	$1.8x10^{18}$
63	140	100/0.3	120	56	10.6	$6.9x10^{15}$
61	88.1	100/2.0	120	2.4	3.3	$7.6x10^{17}$
62	98	100/2.0	120	33.5	12	$1.7x10^{16}$
70	81.5	100/4.0	120	0.3	1.6	$1.2x10^{19}$

Figure Y5.2. displays the x-ray diffraction spectra of two films deposited on PEN substrate and one deposited and annealed on glass. Only peaks associated with the PEN substrate is observed, while no peak is observed on the film on glass, indicative of the amorphous nature of the films.

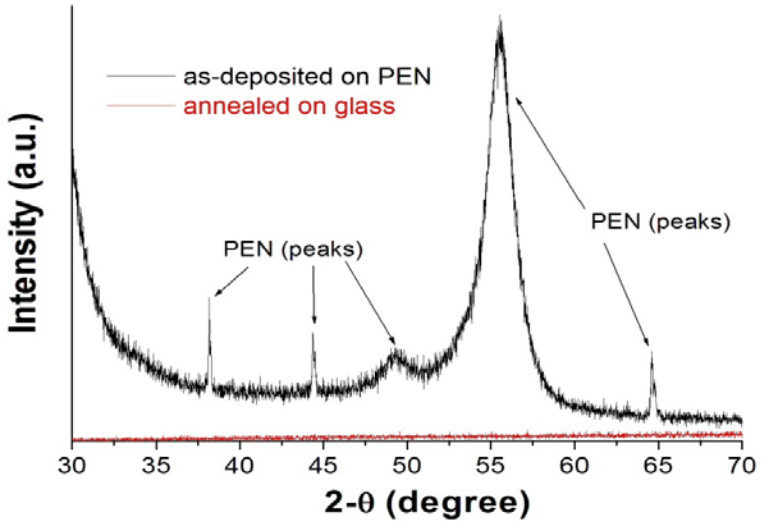


Figure Y5.2. X-ray diffraction of as-deposited GSZO film on PEN and annealed GSZO film on glass.

Numerous TFTs of various structural layouts were fabricated by conventional photolithography on Si. Thermally grown SiO_2 of thickness 200 nm was used as the gate oxide.

Ti/Au metals were used for drain and source contacts. Silver paste applied to the conductive silicon substrate served as the gate contact.

The three TFT structures used are illustrated in Figure Y5.3. The first structure is a simple bar that allows for electrical evaluations, without the structural issues introduced by a more complex design. The effects of increasing the W/L ratio are explored by using the second structure. This interdigitated design is a space efficient way to increase the width without occupying significant space on the photomask. The third structure examines the effects of source/drain design.

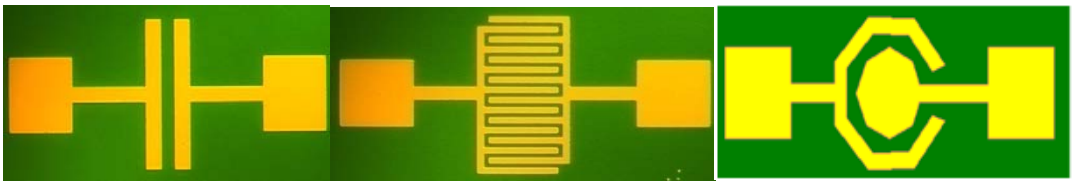


Figure Y5.3. TFT source/drain contact's structural layouts.

The Keithley 4200 model semiconductor parameter analyzer was used to obtain the transfer and output characteristics of the devices. All the TFTs were subjected to annealing in either air or vacuum for 4 hours based on our studies carried out above. It was found that only the air-annealing produced better current on/off ratio and transistor characteristics. Figures Y5.4(a)-(c) and Y5.5(a)-(c) exhibit, output, variation of currents with gate voltage and transfer characteristics on the TFTs annealed in air for 4 hours before and after the metallization, respectively. The field effect mobility was calculated from the slope of the transfer characteristics (Figures. Y5.4(c) and Y5.5(c)) as indicated by

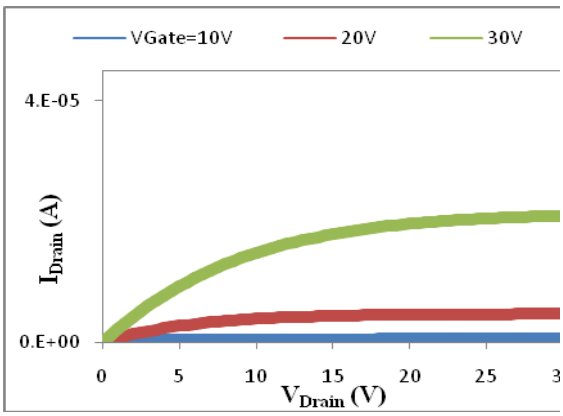
$$I_D = \frac{W}{2L}\mu_{sat}C_{ox}(V_{GS} - V_{TH})^2$$

$$\mu_{sat} = \frac{\left(\frac{2L}{WC_{ox}}\right)I_D}{(V_{GS} - V_{TH})^2}$$

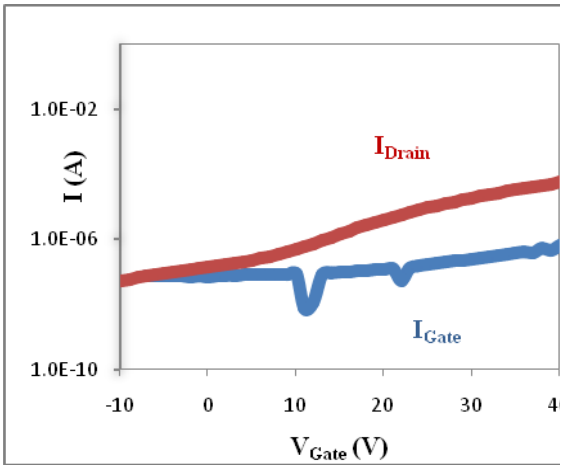
$$Slope = \frac{\sqrt{I_D}}{(V_{GS} - V_{TH})}$$

$$\mu_{sat} = \left(\frac{2L}{WC_{ox}}\right)Slope^2$$

The current on/off ratio is improved on the TFT with annealing carried out after metallization. This was found to be true for all three layouts examined.



(a)



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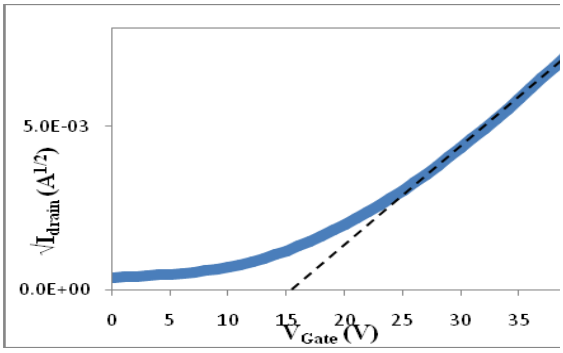
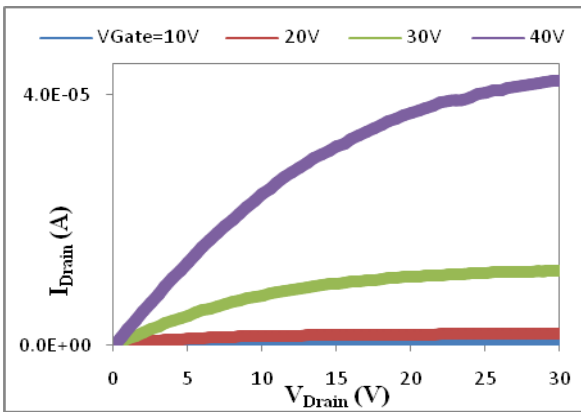
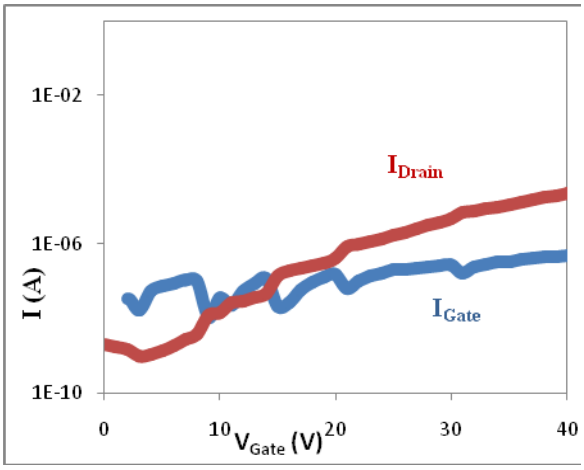


(c)

Figure Y5.4. GSZO TFT with pre-metalization - (a) output characteristics, (b) transfer characteristics and (c)threshold voltage.



(a)



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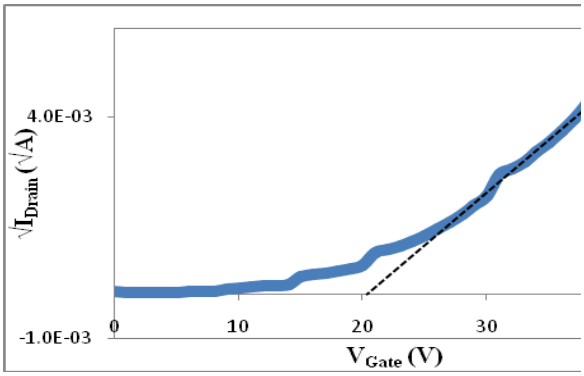


(c)

Figure Y5.5. GSZO TFT with post-metalization annealing- (a) output characteristics, (b) transfer characteristics and (c) threshold voltage.

Figure Y5.6. indicates the variation in the current on/off ratio and the mobility for the three layouts. The interdigitated finger lay out seems to exhibit a better current on/off ratio than the other layouts with comparable mobility values.

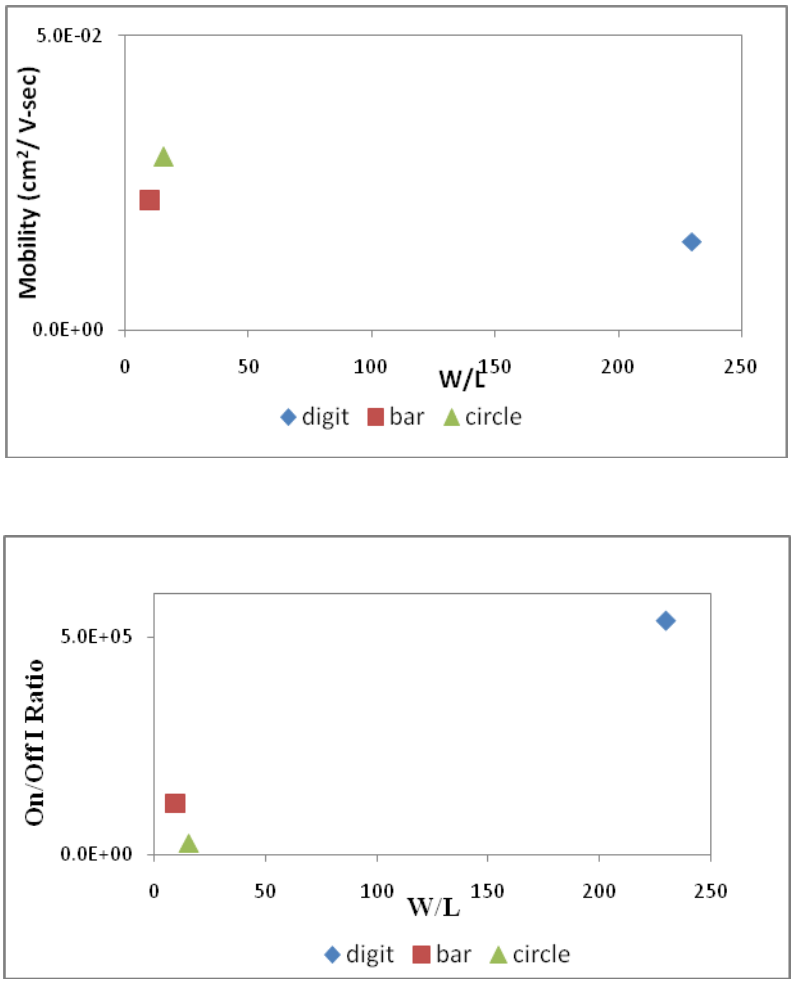


Figure Y5.6. Electrical characterization vs. W/L ratio.

There are only two reports[13,14] on the GSZO TFT. Fortunato et al.[13] reports on a TFT composed of GSZO deposited at room temperature and annealed at 300 °C that yields a saturation mobility of 18.1 cm^2/V-sec, threshold voltage of 6.5 V, 10 µA on current and an on/off ratio of $2x10^7$. Similarly, Ogo et al.[14] produced a TFT also with films deposited at room temperature and annealed at 300 °C yielded a mobility of 10^{-2} cm^2/ V-sec, threshold voltage of 2.5 V, 10 nA on drain current and an on/off ratio of $<10^3$. When compared to the referenced literature, our TFT's performance falls in the middle of the two. Our films were annealed at 250 °C yielding a TFT with a mobility of $2x10^{-2}$ cm^2/ V-sec, threshold voltage in the range of 15-20 V, 20-40 µA on current, and an on/off current ratio of $5x10^5$. One problem was the large gate current observed in these structures indicative of an inferior quality of the gate oxide grown. These were

the preliminary data and no optimization had been carried out on the gate oxide growth or on the TFT processing and annealing parameters, indicating potential for improvement. This work was accepted for oral presentation at MRS Fall 2009 Conference at Boston[15].

iii. Infrastructure Development

Materials and Device Stability Testing Systems

(a) Device Stability System

A device stability testing system was set up. This system was used to visually record the degradation of the devices over time, under bias conditions in the devices, namely organic light emitting diodes (OLEDs), and materials such as ZnO and GSZO, under bend testing. This system may have more applications in the future.

The system essentially consists of an automated digital camera connected to a computer, computer software, a mechanism for mounting the camera, and automated measurement of electrical characteristics. The Canon Powershot A590 camera was used, which replaced older version Canon Powershot A520 as the former had higher resolution images. Enhanced zoom and macro focuser attachments were utilized to ensure the maximum quality of our images.

The software that was used to interface with the camera was also a Canon product, called *ZoomBrowser*. Attempts were made initially to write VisualBASIC programs to interface with the camera via a USB cable, but it was quickly realized that it would be more time efficient to use the software that was included with the camera from Canon. Most importantly, it already had a function built-in to automate that shutter on the camera, so that images could be captured at fixed time intervals.

Testing of OLEDs and hybrid light emitting diodes (HLEDs) were the initial impetus for the development of this system. However, since the success of the system with OLEDs, potential for applications with other devices has emerged. A schematic diagram and photograph of the setup for measuring the degradation of OLEDs over time is shown in Figures. Y5.7 and Y5.8 respectively. As shown, the digital camera is connected to a standard Dell desktop computer with a USB cable. A constant current source is used to stimulate the OLED, causing it to illuminate. The voltage between the anode and cathode of the OLED is measured using a device called a Lab Pro. The Lab Pro has voltage probes that clip to the OLED. It is essentially an analog to digital converter, which converts

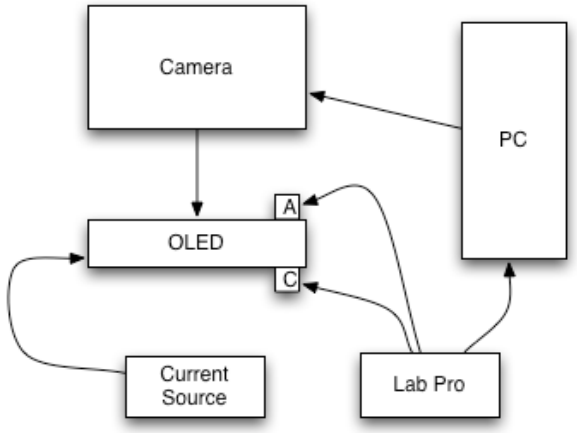


Figure.Y5.7. Diagram of the system for testing OLED degradation.

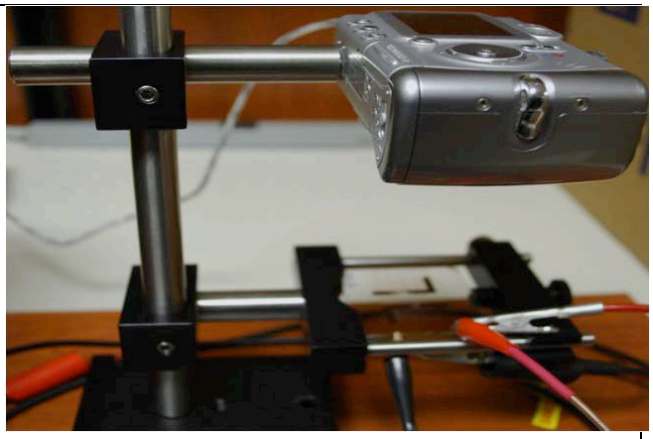


Figure.Y5.8. Photograph of the system for testing OLED degradation. In the upper portion of the image, the old Canon Powershot A590 is shown, pointing downwards to the OLED (L-shaped metal on glass). The wires connected to the contant current source and Lab Pro device are in the lower right corner. The USB cable leading to the PC can be seen in the background.

The analog voltage signal from the OLED to a digital signal to be read by the PC. The software was configured to send a signal to the camera on a specified time interval, causing the camera to take a picture and send the photograph back to the PC. The computer records the photograph and voltage data of the degrading OLED in real time. The OLED begins to degrade as soon as the constant source of current is applied to it. The degradation causes the internal resistance of the device to change. Since the current applied is a constant, from Ohm's Law, $V_{A-C}=I_{source}R_{OLED}$, the voltage between the anode and cathode of the OLED will be proportional to the resistance of the OLED. The PC was set-up to record the photographs of the OLED and the voltage across the OLED, as it degraded over a period of 200 hours. Figure Y5.9 shows color-inverted images from the photographs taken and Figure. Y5.10 shows the voltage vs. time plot for the same OLED. This plot was generated in real-time as the OLED degraded, with each new data point generated from the digital voltage signal produced by the Lab Pro device. There is a gap in the data between the times of 70 and 130 hours, because the system was being reconfigured during that time, which led to the increased resolution in the data seen after the gap. The linear increase in the voltage over time indicates that as the OLED degrades the internal resistance of the OLED increases linearly with the voltage.

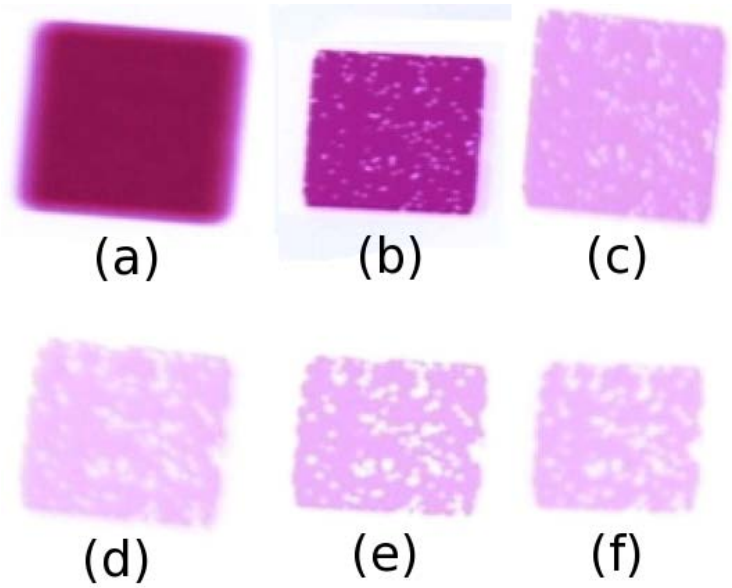


Figure Y5.9. Color-inverted, sequential photographs of the degrading OLED. (a): The OLED has not yet degraded and appears brightly lit. (b): The OLED has begun to degrade, showing small spots absent of illumination. (c): The OLED has degraded further, showing more spots. (d): The OLED is considerably dimmer and has pronounced spots. (e): The OLED no longer has clear edges and has patches absent of illumination. (f): The OLED has continued to degrade.

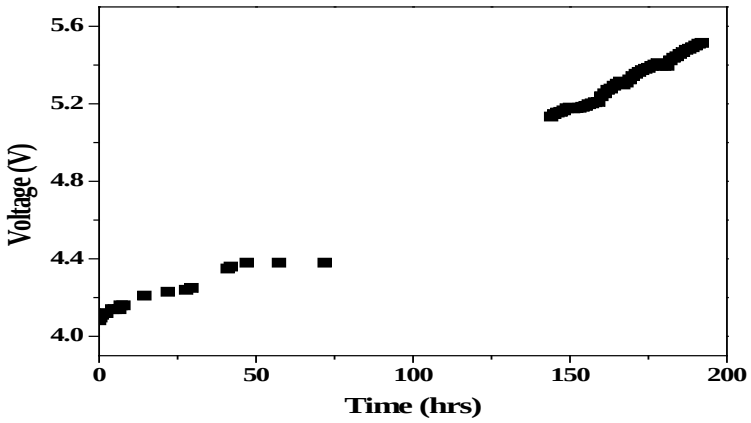


Figure Y5.10. Plot of voltage vs. time for the OLED.

(b) Material Test System under Bend Testing

A schematic for the system is currently being developed for recording the integrity of ZnO and its alloys during the bend testing as shown in Figure Y5.11. In this system, the PC sends a signal to the camera which is attached to the microscope. The PC sends a signal to the camera to open the shutter on a regular interval of time, the light reflected off of the films is focused and magnified by the microscope and captured by the camera. Thus, the camera is being automated to take photographs through the Olympus BX60M microscope, of the cracks developing in-situ during the bending of the films. An adapter was identified, that would fit the port called the "Trinoc"' port of the microscope (Figure Y5.12). As this is a very specialized item there has been a problem in getting the right adapter.

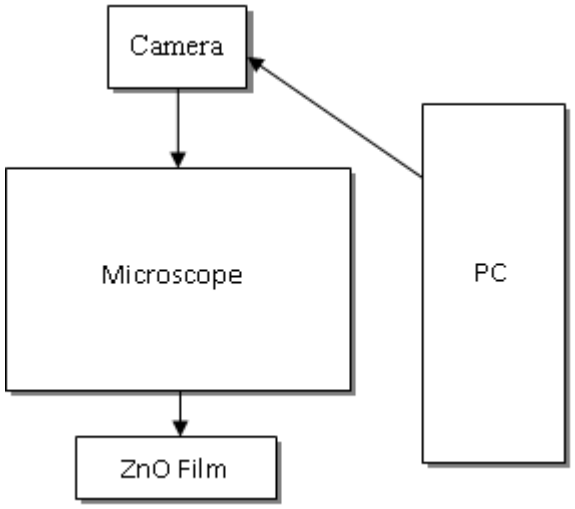


Figure Y5.11. Diagram of the system using the Olympus microscope to photograph material.

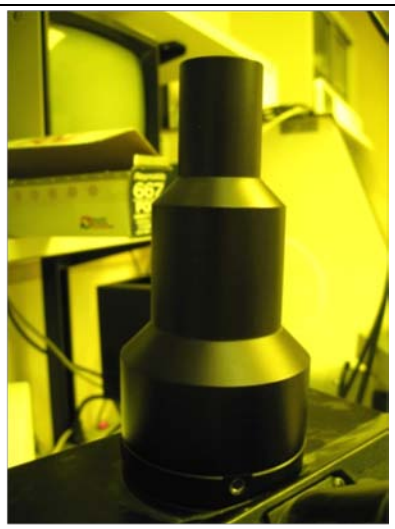


Figure Y5.12. Photograph of the "Trinoc" port of the Olympus microscope, for which an adapter is required to attach the Canon camera.

In conclusion, the system for documenting the degradation of OLEDs over time has been successful. There has been a considerable delay in developing the system for testing the stability of material system with the Olympus microscope as the vendor provided a wrong size adapter for attaching the camera. A replacement adapter from Zarf Enterprises has been placed under order.

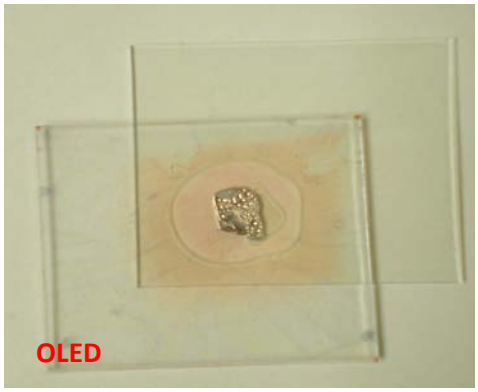
iv. Student Participation and Educational Component

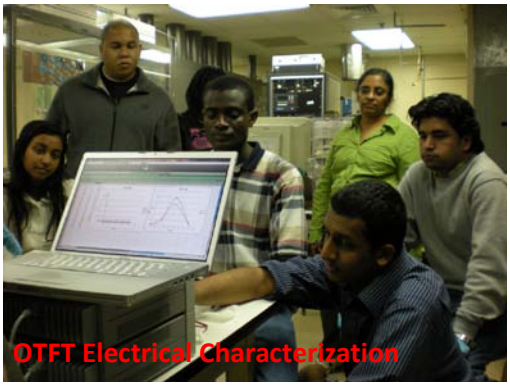
The funding supported two undergraduates, three M.S.E.E. students, one Ph.D. candidate partially, one postdoctoral research associate, and the PI. Two M.S.E.E. theses entitled "The optical and mechanical properties of ZnO:F thin films deposited onto polyethylene napthalate and glass" and "The structural and **e**lectrical properties of RF sputtered ZnO:F thin films deposited on polyethylene naphthalate and glass" by **Stan Potozny**[10] and **Adam Bowen**[12] were completed

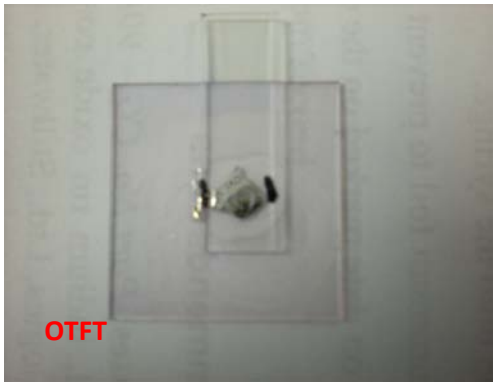
during this period. **Eric Forsythe** from ARL and Jay Lewis from RTI served on their thesis committee, respectively. Supplemental funding was provided for five summer interns to work at NCA&TSU, RTI and ASU. **Tanina Bradley**, a doctoral student was relocated to Research Triangle Park, North Carolina to continue our ongoing investigation on TFT development at RTI with Jay Lewis. An undergraduate **Rahsaan Mitchel** summer interned at ASU and worked under the guidance of **Terry Alford's** group on examining the surface morphology of ZnO:F films and mechanical testing of the films provided by his group. He was also trained on Hall measurements. Three of the M.S.E.E. students **Adam Bowen**, **Robert Alston** and **Jonathan Poe** continued their research work at NCA&TSU on sputtered films and developing device stability testing systems.

The manuscript on MBE grown III-V alloys was *accepted for publication*[2] *in J. Vac. Sci. Tech. B* and a manuscript[10] on ZnO:F sputtered films with the M.S.E.E. student Adam Bowen as the first author was in preparation. There were *three presentations*[16-18] made by the students at MRS/AVS/ASM NC Section Fall Meeting 2008 at Raleigh, MRS Fall Meeting at Boston, Fall 2008, 8th Annual Flexible Electronics & Display Conference, Phoenix, Feb. 2009 AZ, and one has been accepted for oral presentation[15] at MRS Fall Meeting at Boston, Fall 2009. There were also three poster[19-21] presentations by the students at the BCE annual review meeting, held in April 2009, as a part of the review process.

Dr. Michael Escuti and his Ph.D. student Mr. Brandon Conover from Electrical and Computer Engineering, NCSU, Raleigh set up and administered two laboratory modules on Organic Thin Film Transistor and Organic Light Emitting Diode, as a laboratory component for the ELEN 801 course entitled "Semiconductor Devices" taught by Dr. Iyer. The laboratory modules were set up in the Microelectronics Fabrication Laboratory at McNair Hall 140 on 02/27/09 and the two labs were successfully carried out from 9am -4pm. By the end of the day each of the six students was able to fabricate a working organic TFT and LED device**.**







Year 6

i. Transparent Amorphous Oxide Semiconductor TFTs

RF sputtered films of gallium tin zinc oxides (GSZO) have been the main focus of this funding period, in collaboration with RTI. The processing of TFT fabrication was transitioned from RTI to NCA&TSU during this period. TFTs with amorphous GSZO channel layers were deposited using radio-frequency (RF) sputter deposition. The effects of deposition conditions were investigated to reduce oxygen vacancies and improve surface morphology. Post-annealing was performed at various temperatures and durations to decease the resistivity of the channel. Bottom gate TFTs were fabricated using annealed GSZO channels on thermally grown silicon dioxide (SiO_2) on p-Si wafers. The TFTs produced demonstrated good preliminary electrical performance characteristics. The fabrication and systematic optimization processes were carried out as functions of deposition parameters, oxygen flow rate, post-deposition annealing conditions and device parameters, namely channel width/length ratio and source/drain design.

(a) XRD, Hall and AFM Results on GSZO Films

GSZO films were deposited on Corning 7059 glass at various powers and then annealed for 4, 8 and 12 hours in rough vacuum at 200 °C. XRD was utilized to verify the amorphous nature of the as-deposited films and observe crystalline peaks, if any, at longer annealing durations. XRD results performed on films deposited onto 7059 glass are shown in Figure Y6.1. Films annealed for durations of 8 and 12 hours, along with bare, as-deposited GSZO films on 7059 glass substrates were investigated. There is a slight difference observed between XRD results performed on the bare substrate and the annealed films. The as-deposited glass substrate exhibits sharp peaks due to the sample stage used for XRD measurements. A peak at 30° for the 8 hrs annealed films suggests the films are slightly crystalline, and increases in crystallinity as annealing duration in vacuum increases. Figures Y6.2a & b show results of resistivity (ρ) and Hall mobility (μ) values measured from the deposited GSZO films as functions of annealing durations. Figure Y6.2b shows that ρ values vary slightly as annealing durations increase with values as low as 2Ω-cm. Figure Y6.3a shows that mobility μ values decrease as annealing durations increase. The GSZO film deposited at 100 W yielded a Hall μ of 3cm^2 $V^{-1}s^{-1}$.

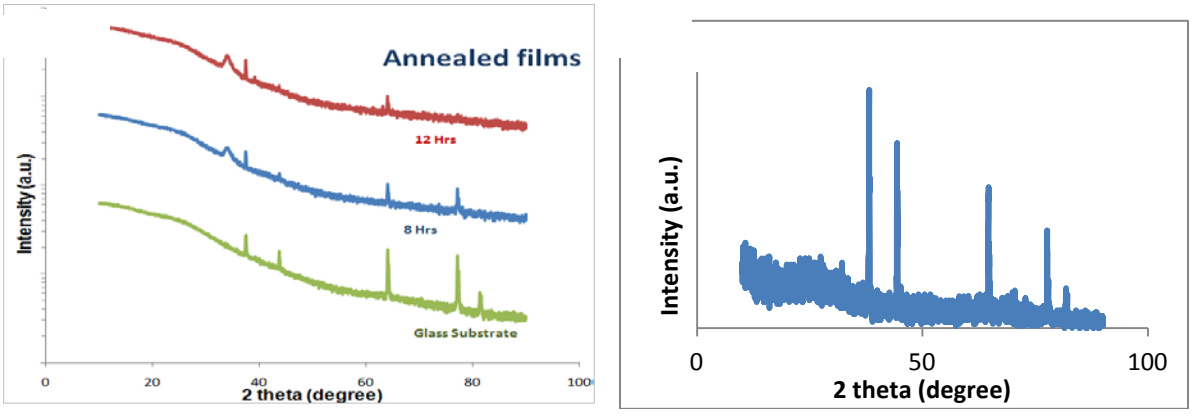


Figure Y6.1. XRD of (a) GSZO on 7059 glass and (b) sample holder stage.

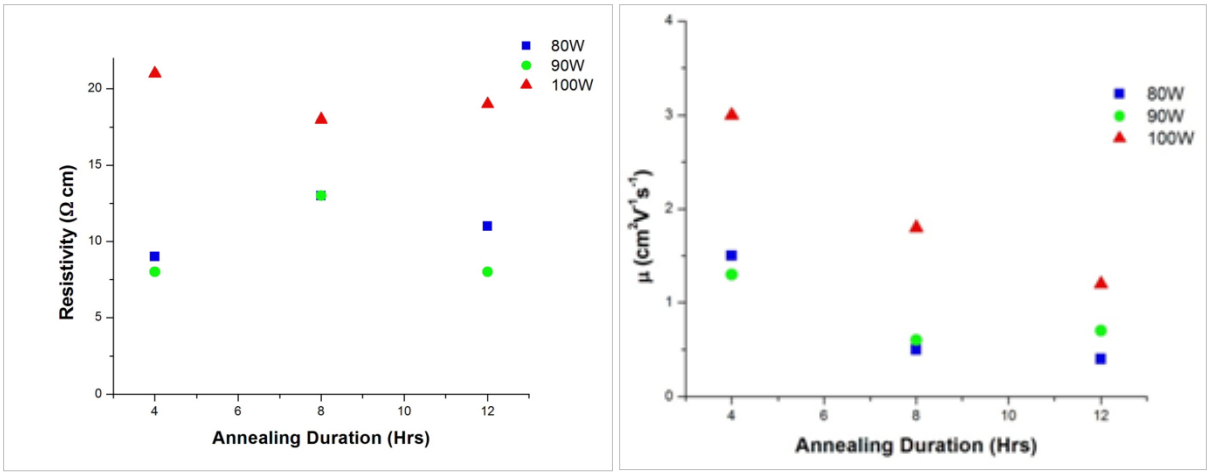
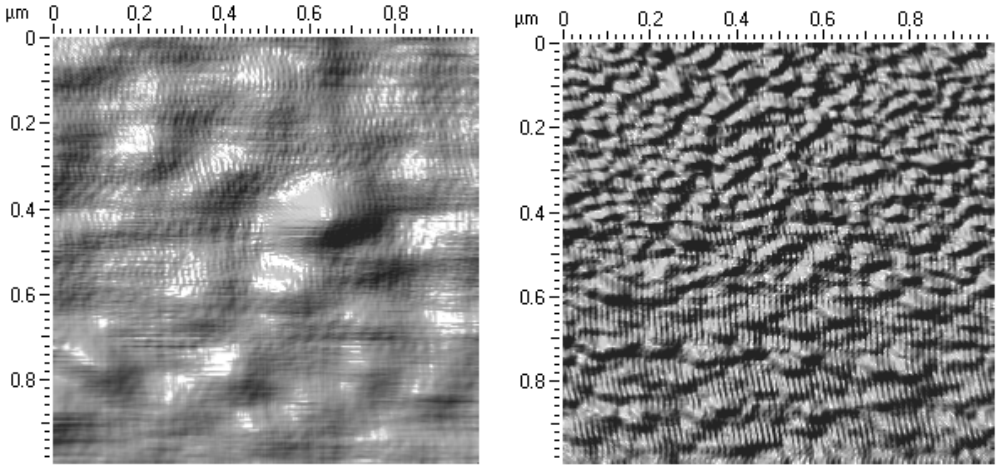


Figure Y6.2. (a)Resistivity and (b)mobility values measured by the Hall technique.

TFTs were initially fabricated with SiO_2 gate dielectrics produced by plasma enhanced chemical vapor deposition (PECVD). These TFTs exhibited high gate leakage, which will be shown in the following section. AFM was used to examine the surface roughness of GSZO deposited on both PECVD and dry oxidation produced SiO_2. The AFM images of Figure Y6.3. shows a larger grain size for the films on PECVD SiO_2. The surface roughness as a result of oxygen partial pressure during deposition was also investigated and showed a slight increase in roughness with higher oxygen flow (Figure Y6.4).



1x1 magnification 012610 GSZO~36.6nm Si/SiO_2 450C 1hr Air-ann Ra=8.97Å PECVD

1x1 magnification 021010 GSZO~134nm Si/SiO_2 450C 1hr Air-ann Ra=5.36Å thermal oxide

Figure Y6.3. AFM of (a) GSZO on PECVD SiO2 and (b) GSZO on thermally grown SiO_2 by dry oxidation.

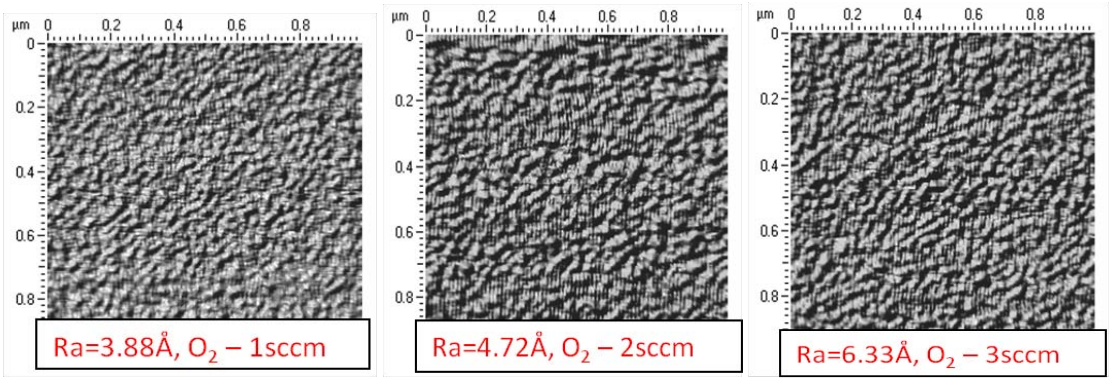


Figure Y6.4. AFM of GSZO deposited at various oxygen flow rates.

(b) Resistivity Measurements by Transmission Line Method

As Hall measurements are difficult to perform on high resistivity GSZO films, transmission line measurements are being utilized to measure the sheet resistance of the films, electrode specific contact resistivity and contact resistance. A pad of 7x7 mm^2 with different inter-electrode distances (L) were patterned using the conventional photolithographic process on 33 nm thick GSZO films deposited on a glass sample of size 50 X 50 mm^2 and annealed at 250 ^{o} C for 1 hour. An electron beam evaporated Al metal layer of thickness 207 nm has been used as the contact material for the pad. For preliminary investigation Al is being used in place of Ti/Au to cut down on the cost, and will be switched to the Ti/Au contacts once the process is standardized]. The standard "lift off" process was used to remove the metal deposited on the photoresist in between the electrodes. Figure Y6.5 shows the three layers of contacts used for measuring the contact resistance using TLM. Figure Y6.6 shows the plot of the measured values of the resistance (R) for the bottom layer consisting of five pads as a function of L.

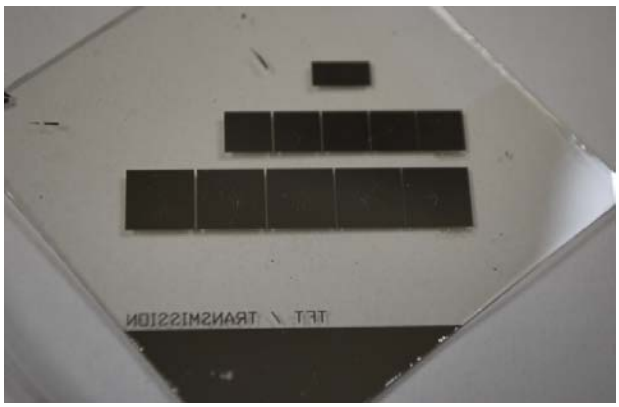


Figure Y6.5. Image of pattern in measuring contact resistance by TLM

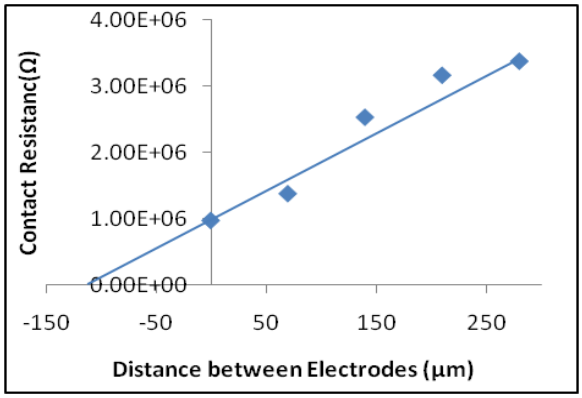


Figure Y6.6. Variation of resistance with length of Al contact pads

TLM analysis yields the following equations[1]:

$R(L) = (R_{sheet} / W)(L+2L_T)$.....1.1

$R(L=0) = 2R_c = (R_{sheet}/W)2L_T$.....1.2

The contact resistance (R_c) and transfer length (L_T) are determined from the y- and x-intercepts (from extrapolated line), respectively. The specific contact resistance (ρ_c in Ω-cm^2) is then computed from the product of the contact resistance with the contact area . R_{sheet} is then computed from equation 1.2, knowing all other parameters. The calculated values are tabulated in Table Y6.1 below.

Table Y6.1 Contact resistance, specific contact resistance, transfer length and sheet resistance from TLM.

L(μm)	L(cm)	$R_{measured}$ (Ω)	Contact Resistance, Rc(Ω)	Specific Contact Resistance, Ω-cm^2	Transfer Length, L_T(cm)	Sheet Resistance R_{sheet}(Ω/□)
0	0	$9.8x10^5$				
70	0.007	$1.4x10^6$				
140	0.014	$2.5x10^6$	$0.5x10^6$	$0.25x10^6$	0.005	7×10^7
210	0.021	$3.2x10^6$				
280	0.028	$3.4x10^6$				

The sheet resistance is quite high and these are just preliminary data and these will be used as a part of regular characterization of the layers in future and will be correlated to the TFT performance of the device.

(c) TFT Performance

Bottom gate TFTs were produced with a GSZO channel layer. A SiO_2 gate dielectric was produced by dry oxidation on a silicon substrate. A blanket layer of GSZO was then deposited primarily at RT, though some were deposited at 150 ˚C. The semiconductor was patterned using a wet chemical etch, while source/drain contacts were patterned by a lift-off process. Prior to metallization, the samples underwent plasma cleaning to remove excess residue from the S/D patterned areas. Titanium and gold films of 10 nm and 100 nm, respectively, were used for the metallization of the S/D contacts. Film deposition parameters, annealing conditions, S/D layout, and post-contact annealing have all been investigated to realize their effects on TFT electrical performance. Initially, our films were annealed in vacuum, this yielded channel layers with low resistivity's, as shown in Figure Y6.2, and TFTs with high gate leakage. After this observation, we began annealing in air and decreased the sputtering power to 45 W to reduce the sputtering damage to the oxide layer. The gate leakage current was reduced significantly but was still high. As mentioned above, three S/D layouts were utilized. Figures Y6.7a, b, &c show output characteristics of various S/D layouts. These graphs show a slight difference in drain current, which can be attributed to the differences in channel width due to the S/D configuration. The most significant difference among the graphs was the obvious saturation of the TFT with the circular layout. When observing the transfer characteristics, there were similar results among the three devices. They showed gate currents approximately one order of magnitude less than the

drain current, which ranged from $6x10^{-6}$ to $9x10^{-6}$ A. All three devices had a current of at least $2.7x10^{-7}$ A at Vg=0, signifying that they were depletion-mode transistors. These TFTs had a gate dielectric of 128 nm and a channel layer thickness of 85 nm. After deposition of the channel layer, they were annealed in air for 4 hours. Figure Y6.8 illustrates the effects of W/L ratio on drain current and on/off ratio. Due to the involved nature of determining the width of the digit and circular layouts, the focus since then has been shifted exclusively to the bar layout.

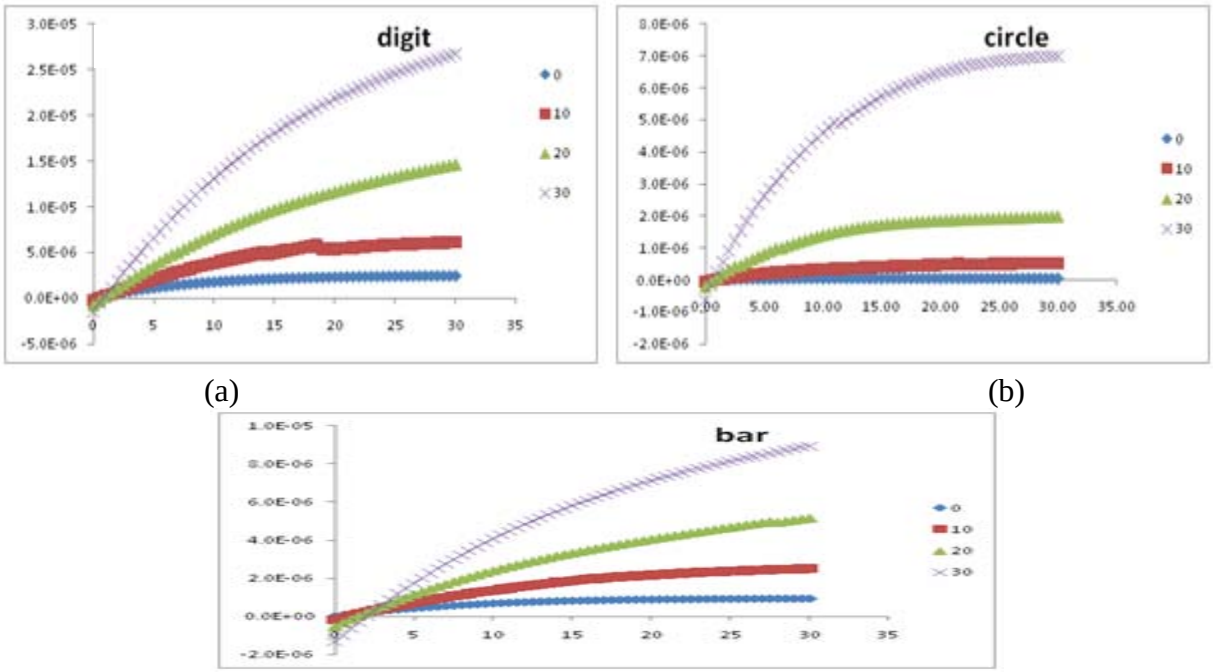


Figure Y6.7. TFT output characteristics of (a) digit (b) circle and (c) bar layouts.

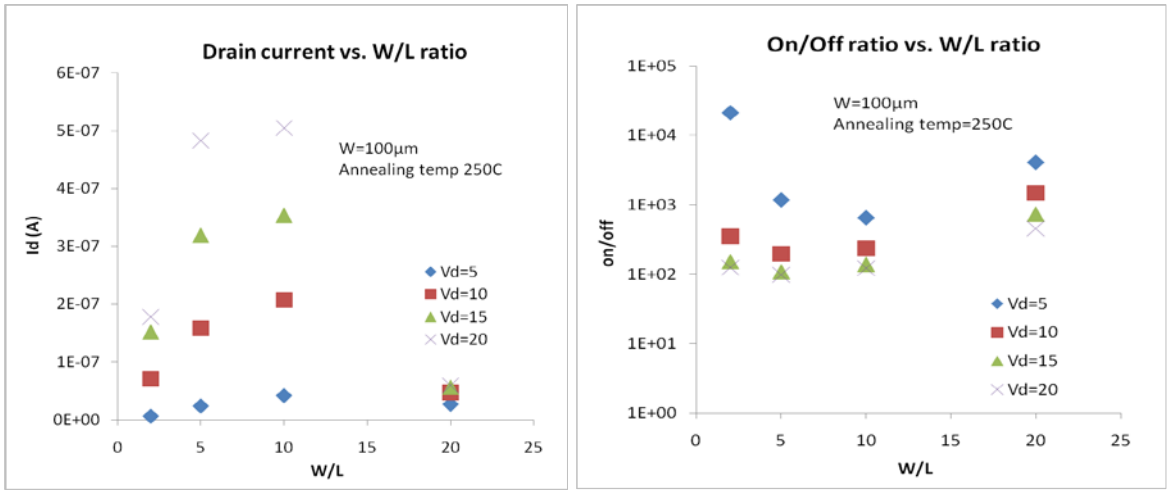


Figure Y6.8. W/L ratio effect of drain current and on/off ratio.

Numerous TFTs were produced with air annealed channel layers that yielded low on/off current ratios (not shown). To remedy this problem as well as reduce gate leakage through defect paths outside the device area, the TFT structure was slightly changed. Instead of placing S/D contacts on a blanket layer of GSZO, the GSZO was etched to isolate each device as shown in Figure Y6.9. The gate contact was placed by scribing through the gate oxide layer to the silicon substrate and applying silver paint. The modification resulted in pinch off region occurring at a lower voltage and drastic reduction in the gate current, as displayed in Figure Y6.10.

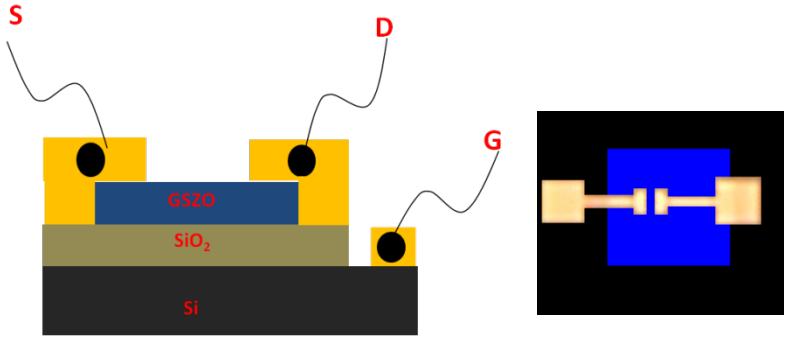


Figure Y6.9. TFT cross section and S/D layout with GSZO isolation.

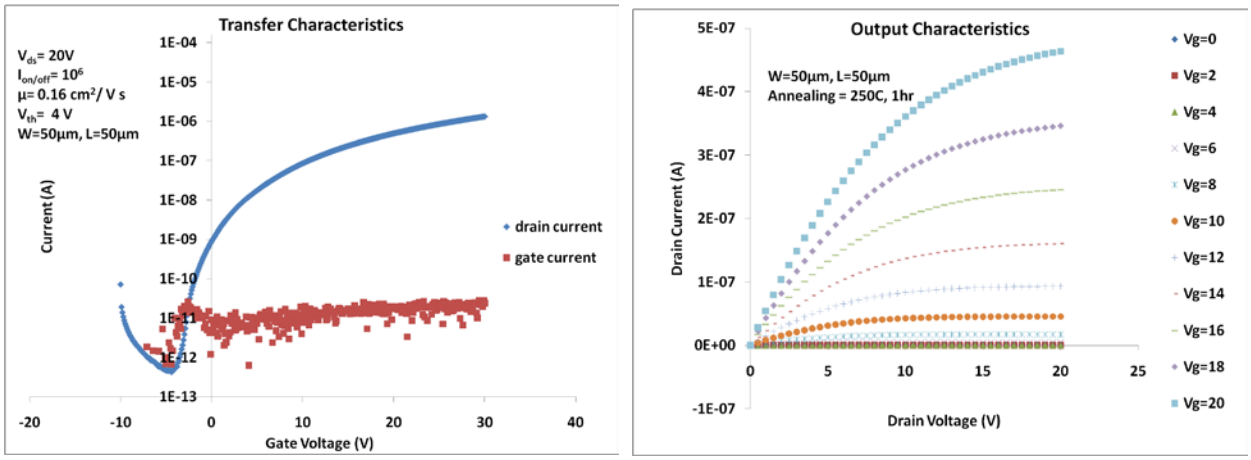


Figure Y6.10. TFT results with GSZO isolation.

The effect of an elevated deposition temperature was also investigated. We have fabricated TFTs with GSZO channel layers deposited at RT and an ET of 150 °C. Relatively small μ_{sat} have been observed in both sets of TFTs, suggesting the existence of electron traps located in the semiconductor to oxide interface. The highest μ_{sat} was observed for samples annealed at 450 °C for 15 minutes, suggesting that higher thermal energy reduces scattering defects located within the semiconductor and at the semiconductor/oxide interface. It is assumed that thermal excitation induces atomic rearrangements involving the displacement of oxygen ions to remove electron traps. Consistent with literature, $I_{on/off}$ was shown to be approximately 10^6 for most samples. Improved $I_{on/off}$ is indicative of reduced defects located within the oxide. With an increased annealing duration at 250 ^{o}C for 1hr, V_{th} is reduced, suggesting a reduction in the density of trap states localized below the conduction band. Output characteristics of TFTs with RT

& ET GSZO channel layers annealed at 250 °C for 1 hour exhibit good saturation. TFTs with RT & ET GSZO channel layers annealed at 250 °C for 15 minutes and 450 °C for 15 minutes exhibit poor saturation, probably due to a weak channel inversion pinch-off. Figures Y6.11-Y6.114 show results of TFTs produced with various deposition & annealing temperatures and annealing durations. Figure Y6.15 shows the transfer characteristics of the various TFTs for comparison. The field effect mobility (μ_{FE}) and threshold voltage (V_{th}) in the saturation region (V_{ds}=20 V) were calculated by fitting a straight line to the plot of the square root of I_d versus V_g, according to the expression for a field-effect transistor, where W is the width of the channel layer, L is the length of the channel layer and C is the capacitance per unit area of the gate oxide.

$$I_{DS} = \left(\frac{\mu_{FE} WC}{2L}\right)(V_{GS} - V_{th})^2$$

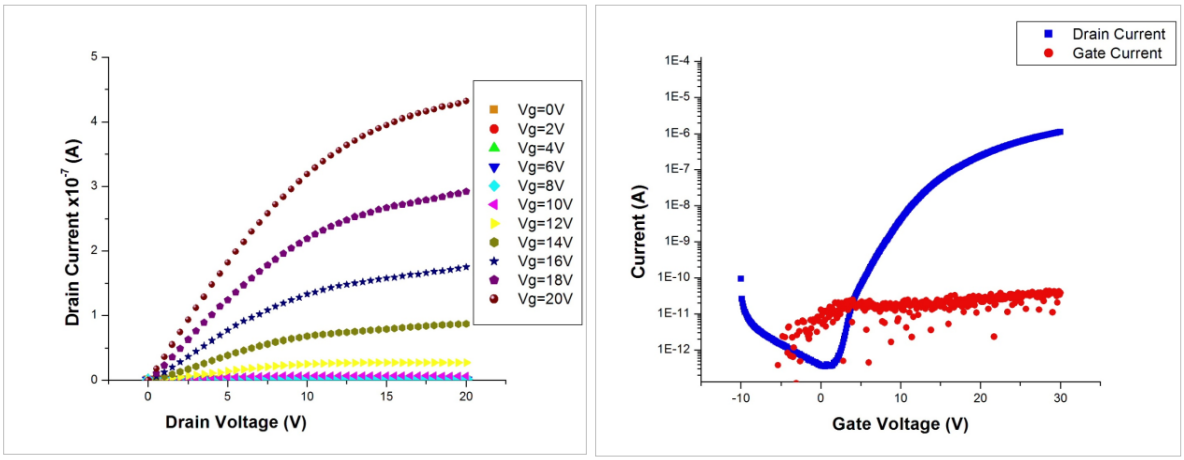


Figure Y6.11. RT GSZO TFT annealed in air at 250 °C for 15 minutes with 2 sccm O_2 flow rate.

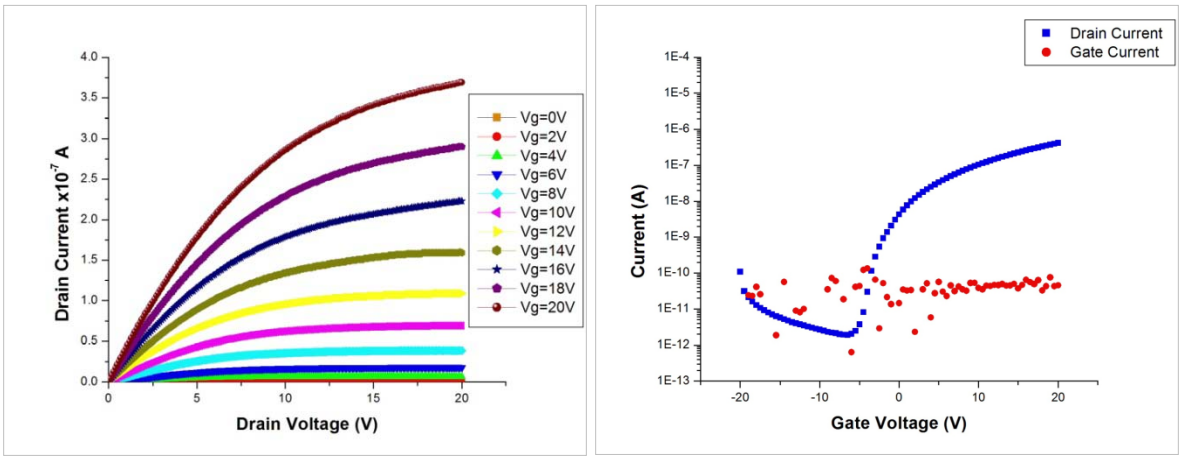


Figure Y6.12. ET GSZO TFT annealed in air at 450 °C for 15 minutes with 2 sccm O_2 flow rate.

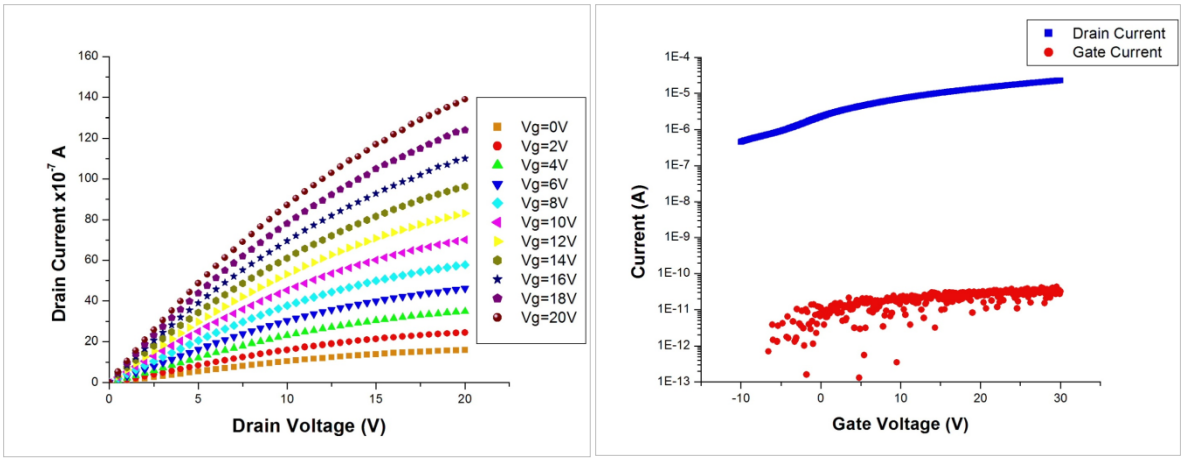


Figure Y6.13. RT GSZO TFT annealed in air at 450 °C for 15 minutes with O_2 flow rate of 2 sccm.

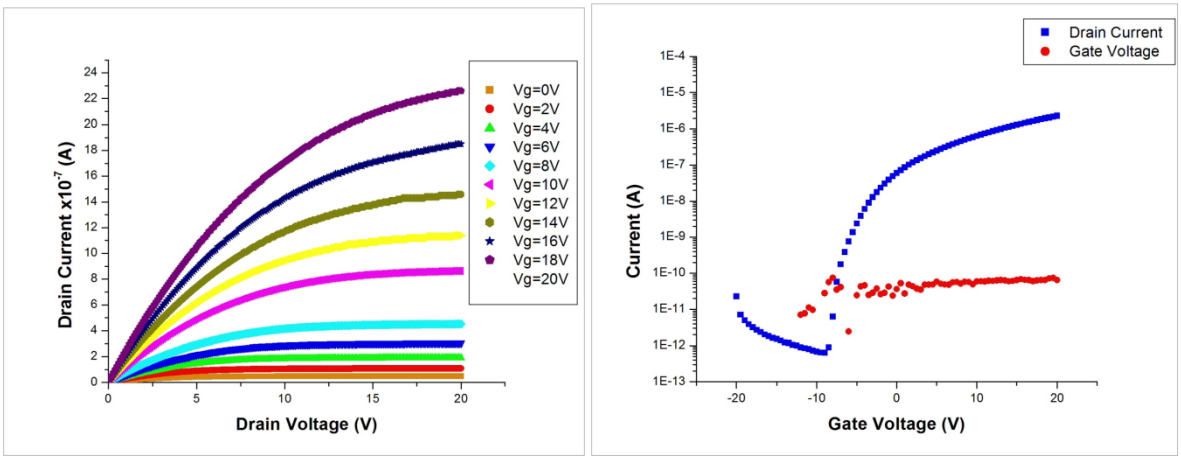


Figure Y6.14. ET GSZO TFT annealed in air at 250 °C for 15 minutes with O_2 flow rate of 2 sccm.

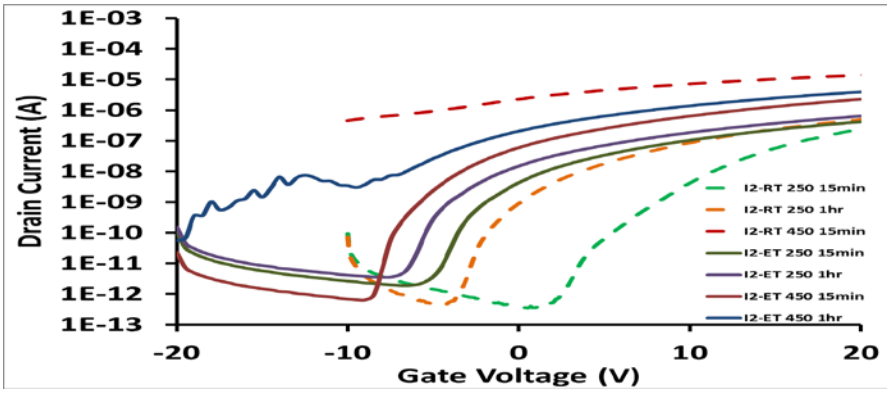


Figure Y6.15. Transfer characteristics of TFTs with various deposition/annealing conditions.

It was noticed that the threshold voltage shifted in the negative direction with higher annealing temperatures. An observation of interest is that the TFTs with films deposited at RT underwent a greater V_{th} reduction shift as opposed to those of ET. This can be attributed to some film defects being passivated during ET deposition, therefore reducing the effects of post deposition annealing. Tables Y6.2 and Y6.3 show the results of RT & ET deposited channel layer TFTs, respectively.

Table Y6.2. TFT results of RT deposited channel layers.

RT						
	Ann Temp(°C)	Ann Dur (min)	V_{th} (V)	on/off ratio	I_d in A @ V_{ds}=20V	I_g in A
	250	15	11	$3.2x10^{6}$	$1.1x10^{-6}$	$1.0x10^{-11}$
	250	**60**	**4**	**$1.3x10^{6}$**	**$1.3x10^{-6}$**	**$1.0x10^{-11}$**
	450	15	-14	N/A	$2.0x10^{-5}$	$1.0x10^{-11}$

Table Y6.3. TFT results of ET deposited channel layers.

ET							
	Dep Temp(°C)	Ann Temp(°C)	Ann Dur (min)	V_{th}	on/off ratio	I_d in A @ V_{ds}=20V	I_g in A
	150	250	15	-1	$2.2x10^{5}$	$4.3x10^{-7}$	$5.0x10^{-11}$
	150	250	60	-2	$1.8x10^{5}$	$6.4x10^{-7}$	$5.0x10^{-11}$
	150	450	15	-1	$3.6x10^{6}$	$2.4x10^{-6}$	$5.0x10^{-11}$
	150	450	60	-4	$1.3x10^{3}$	$3.9x10^{-6}$	N/A

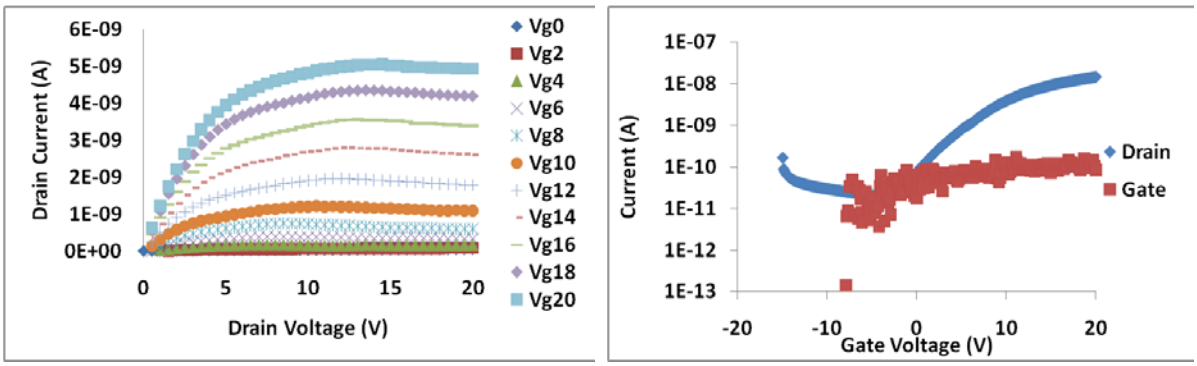


Figure Y6.16. RT deposition, O_2 ~10 sccm, air annealed 250˚C for 15 min.

A reduced drain current is observed with increased oxygen partial pressure (O_{pp}) when comparing Figure Y6.11 with Figure Y6.16. Also, there is a reduction in the drain current on/off ratio with increased O_{pp}. The V_{th} for the TFT in Figure Y6.16 with a value of 1 was less than that of Figure Y6.11, but low V_{th} was not observed with other TFTs produced with the same process parameters. Table Y6.4 shows the TFT results. It is to be noted that in some of the data the I_d in the output characteristics are in error and do not exactly match with those in input characteristics due to the faster scanning speed used in the acquisition of the data.

Table Y6.4. Comparison of typical TFT process parameters with increased O_{pp} parameters.

O_2 sccm	Reference Plot	Ann Temp (˚C)	Ann Time (min)	Ann Ambient	V_{th} (V)	on/off ratio	I_d in A@ V_g=20V, V_{ds}=20V	I_g in A@ V_{ds}=20 V, V_g=20 V
10	Figure 1.18	250	15	air	1	$7.1x10^{2}$	$1.4x10^{-8}$	$8.5x10^{-11}$
2	Figure 1.13	250	15	air	11	$3.2x10^{6}$	$2.4x10^{-7}$	$2.5x10^{-11}$

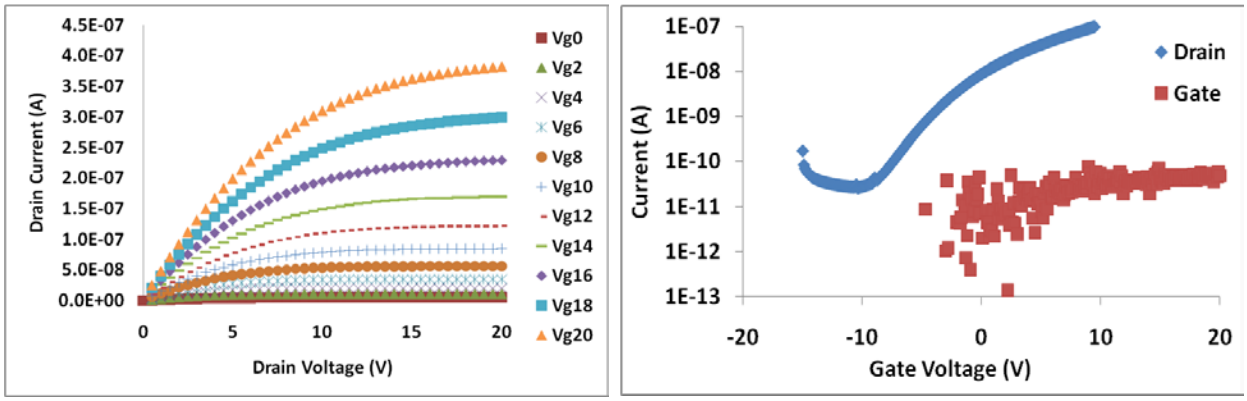


Figure Y6.17. RT deposition, O_2 ~10 sccm, air annealed 300˚C for 15 min.

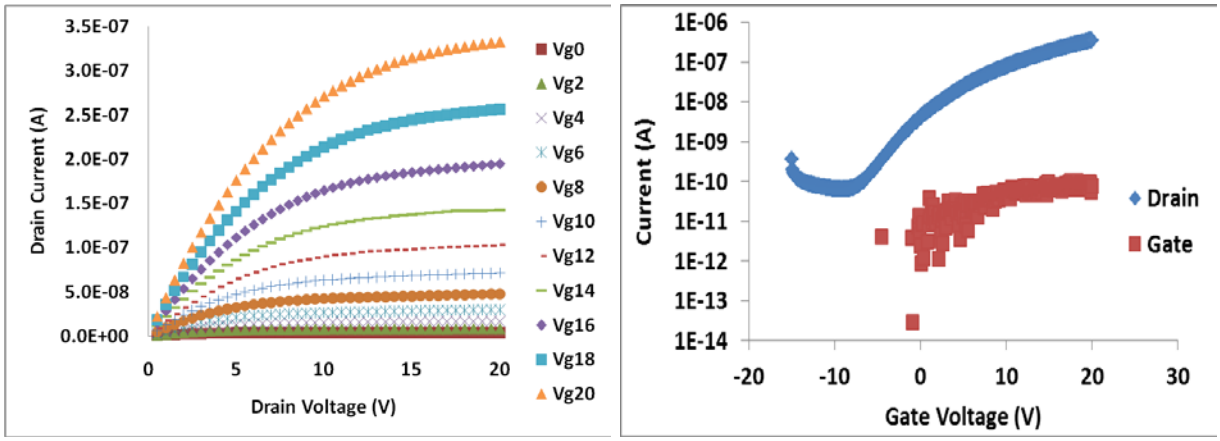


Figure Y6.18. RT deposition, O_2 ~2 sccm, air annealed 300˚C for 15 min.

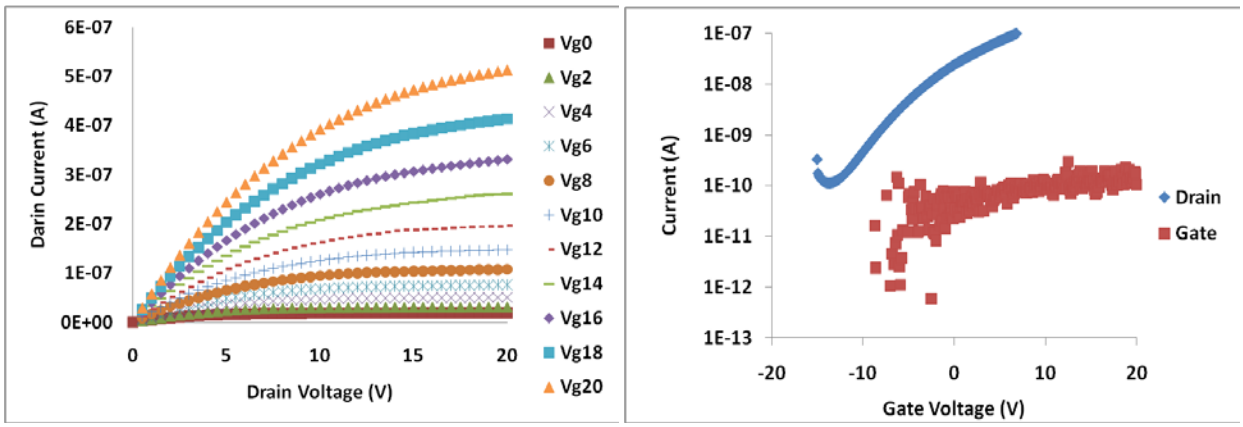


Figure Y6.19. RT deposition, O_2 ~2 sccm, N_2 annealed 300˚C for 15 min.

The TFT characteristics of Figures Y6.17– Y6.18 are listed in Table Y6.5. There was an increase in the on/off current ratio with increased $O_{pp,}$ shown in the data for Figure Y6.17. Annealing in nitrogen had no significant effect on the on/off current ratio or the maximum current achieved at V_{ds} = 20V & V_g = 20V, however the threshold voltage of the nitrogen annealed sample shifted to a negative voltage. Figure Y6.20 illustrates the TFT V_{th} and I_d characteristics based on annealing temperature and O_{pp}.

Table Y6.5. TFT results from Figure Y6.17 – Y6.19.

O_2 sccm	Ann Ambient	Reference Plot	Ann Temp (˚C)	Ann Time (min)	V_{th} (V)	on/off ratio	I_d in A @ V_g=20 V, V_{ds}=20 V	I_g in A @ V_{ds}=20 V, V_g=20 V
10	air	Figure 19	300	15	2	$1.7x10^{4}$	$1.1x10^{-7}$	$1.3x10^{-10}$
2	air	Figure 20	300	15	1	$6.9x10^{3}$	$4.1x10^{-7}$	$5.3x10^{-11}$
2	N_2	Figure 21	300	15	-2	$4.8x10^{3}$	$5.5x10^{-7}$	$1.0x10^{-10}$

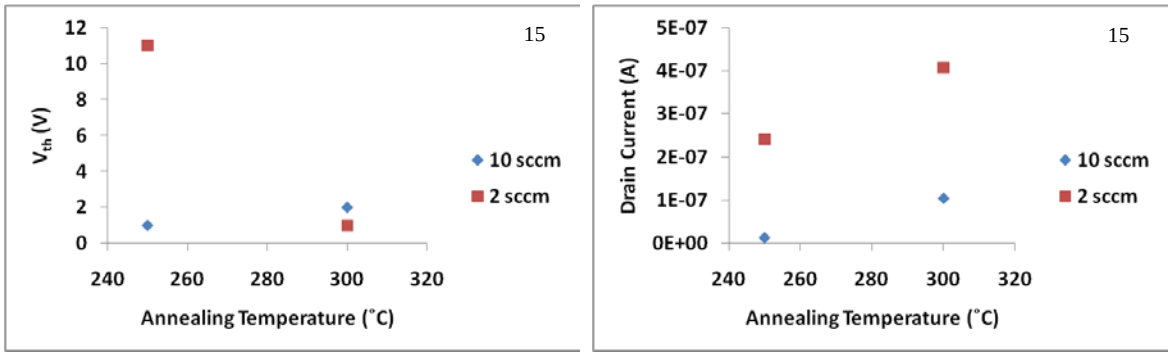


Figure Y6.20. TFT characteristics based on annealing temperature and oxygen pressure.

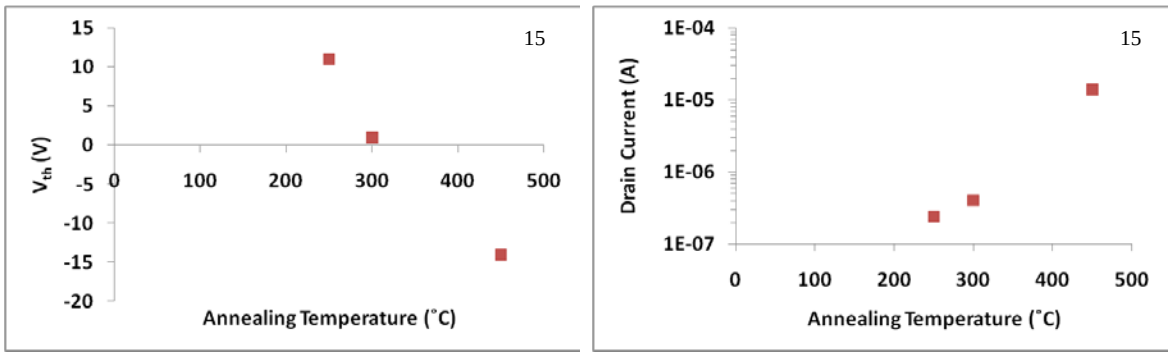


Figure Y6.21. TFT characteristics based on annealing temperature.

(d) Summary

In summary, transparent amorphous films were deposited at NC A&T SU and used as the TFT channel layer. Characterization techniques such as x-ray diffraction, AFM and Hall measurements were performed to assess the structural and electrical characteristics of the deposited films. In addition, the preliminary electrical performance of the TFTs was investigated. The best TFT electrical characteristics with threshold voltage of 4 V and I_d of 10^{-6} A with an on/off current ratio as high as 10^6, have been obtained on RT deposited GSZO channel layers of length and width of 50 µm each, annealed in air at 250 ^{o}C for 1hr. The TFT performance was found to be hindered due to a poor gate oxide, vacuum annealing, excessive annealing times/temperatures, and unintentional GSZO etching. These issues contributed to high gate leakage, device instability, pre-saturation breakdown, and low drain currents. Though some of these issues were resolved, there are still opportunities for significant improvement.

ii. Conclusions

Voltage Threshold

- V_{th} is positive for devices with RT deposition and 250˚C annealing in air.
- V_{th} shifts in the negative direction for devices with ET deposition.
- Variation in V_{th} is a strong function of annealing conditions for layers deposited at RT, while the ones deposited at higher temperature are less influenced by annealing conditions.
- Increased O_{pp} shifts V_{th} in the negative direction.

Drain Current

- Increased O_{pp} during deposition improved pinch-off of the channel and therefore improved the I_d curves' saturation.
- I_d is the highest for the layers annealed at 450˚C.
- I_d appears to be independent of annealing ambient, O_{pp} or the deposition temperature.

On/Off Ratio

- RT deposited layers have greater on/off ratios for shorter annealing durations.

- ET deposited layers have greater on/off ratios for higher annealing temperatures and shorter annealing durations.

From the above preliminary observations and from the literature, we speculate that at higher annealing temperature, higher deposition temperature and annealing in N ambient corresponds to increased oxygen vacancies with increased conductivity. This leads to a negative V_{th}, corresponding to an enhancement mode device with high I_d and low on/off ratio and a depletion mode device can be achieved. V_{th} is positive when oxygen vacancies are low. This is corroborated by layers deposited at different O_2 flow during deposition. The current is low and V_{th} is large and positive for high O_2 pressure and annealing in air.

iii. Student Training and Educational Component

One M.S.E.E. thesis entitled "RF-Sputtered Gallium Tin Zinc Oxide Films and thin film transistors "by Robert Alston[22] and Ph.D. preliminary oral exam by Tanina Bradley[5] were completed during this period. **Eric Forsythe** from ARL and **Jay Lewis** from RTI served on their thesis and dissertation committees, respectively.

The above works resulted in three publications[2,10,23] and a manuscript[24] on GSZO TFT is under preparation to be communicated to a suitable journal for publication. There were two student oral presentations[25,26] made by the students at MRS/AVS/ASM NC Section Fall Meeting 2009 at Raleigh and 9th Annual Flexible Electronics & Display Conference, Phoenix, Feb. 2010 AZ, and two student poster presentations[27,28] were made at MRS/AVS/ASM NC Section Fall Meeting 2009 at Raleigh NC (placed first in the student poster presentation contest).

Tanina Bradley conducted the TFT characterization at RTI, International as semiconductor parameter analyzer was not available in our lab. Also two undergraduate students **Sinelk Behane** and **Jazmin Clark-Harris**, recipients of LSAMP Fellows-2011 worked on measuring the contact resistance of different metal source and drain contacts by transfer length measurement. An oral presentation[29] of this work was made by **Sinelk Behane** at 2011 NC LSAMP/RISE Joint Research Symposium, at Fayettteville State University.

iv. Infrastructure development

Although channel layer deposition has always been performed at A&T, it is to be noted that the processing of all the above TFTs were carried out at RTI international, Inc. Though all the infrastructure for processing was present it was never utilized for research. With the initiation of this research the labs were rearranged and all the equipment such as oxidation furnace, plasma cleaning, metallization, mask aligner, spinner were brought back to operation after conducting few repairs and production of TFTs were carried out successfully in-house. This funding was also leveraged to purchase Keithley 4200-SCS semiconductor parameter analyzer system from the Title III funds. The system was placed on order during this funding period.

The results of our in-house produced TFT are shown in Figure Y6.22. Observation of in-house produced TFT (Figure Y6.22) and comparable RTI produced TFT (Figure Y6.10) shows significant difference in drain current.

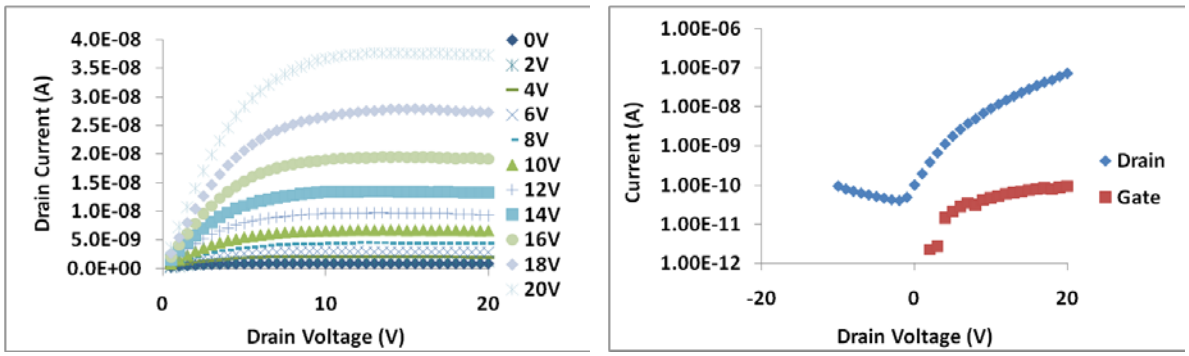


Figure Y6.22. Characteristics of TFTs fabricated in- house.

When examining the in-house produced TFTs under a microscope, GSZO etching was observed (Figure Y6.23). The low currents for the in-house produced TFTs, lack of improvement in TFT characteristics of the RTI produced TFTs and the high film resistivity is attributed to this etching. It is believed that both the NC A&T SU and RTI TFTs suffer from GSZO etching, but to different degrees. To remedy this issue, a thicker layer of photoresist was applied to negate the etching rate of the photoresist developer.

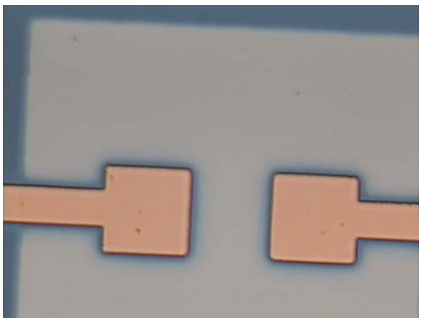


Figure Y6.23. In-house produced TFT with GSZO etching problem.

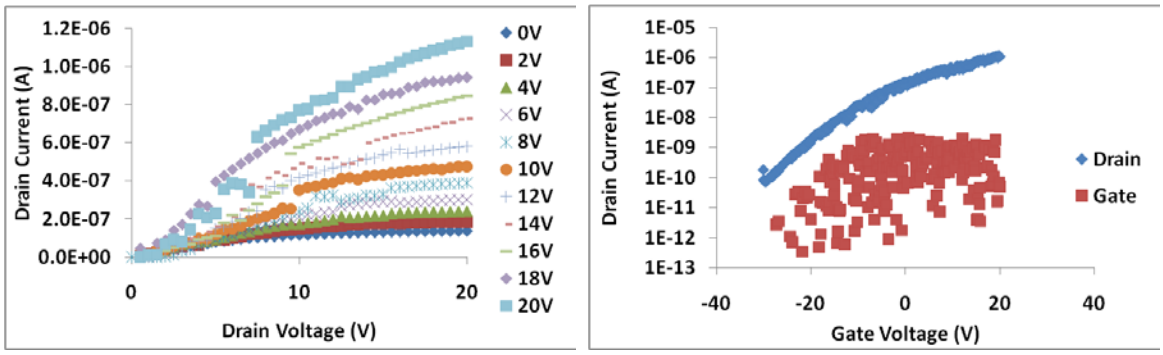


Figure Y6.24. Characteristics of most recently produced, in-house TFTs at 300 ^{o}C for 15 min in air.

TFTs were recently produced after resolving the etching issue. The output and transfer characteristics are shown in Figure Y6.24. Regarding the output characteristics, there are two major differences between Figures Y6.22 & Y6.24. These differences are current saturation and maximum current achieved at V_d=20V and V_g=20V. The TFT in Figure Y6.24 achieves a current of approximately two orders of magnitude higher than that of Figure Y6.22, but Figure Y6.22 shows obvious saturation, signifying a fully pinched off channel, unlike that of Figure Y6.24. The transfer curve's main difference is the shift of the V_{th}. The TFT represented in Figure Y6.22 has a V_{th} of 5V, while that of Figure Y6.24 has a V_{th} of -10V. We believe the poor saturation and negative V_{th} of Figure Y6.24 is attributed to degradation of the channel layer, as it was deposited on 05/28/10 and the resulting TFT was tested on 09/09/10, as opposed to that of Figure Y6.22 where the channel layer was deposited on 07/23/10 and the resulting TFT was tested on 07/27/10.

1.3 Interactions with FDC/ARL

The first component of our research, as mentioned earlier, is a result of an active collaboration with Terry's group at FDC and Eric Forsythe at ARL. The various institutional publication contributors are testimonial to the collaborative nature of our research. Further, for the last few years, quite a few undergraduates have been summer interning and carrying out the Center work with the above two groups. Eric Forsythe served on the thesis committee of Stanley Potoczny, M.S.E.E. and is currently on the dissertation committee of Tanina Bradley, a Ph.D. candidate. Rapid progress in our work would not have been possible but for a positive and active collaborations with FDC/ASU and ARL.

1.4 Scope of Future Work

Annealing effects on semiconductor quality needs further investigation, as these can significantly alter TFT performance. The minimization of interface traps is of interest, along with the use of other dielectrics such as SiN and SiN/SiO_2 stack. Stability testing will be carried out, since device degradation under gate bias stress is one of the major concerns. Interface trap measurement set ups for photo-excited trap-charge-collection spectroscopy and MIS measurements are being developed. The effect of the deposition, annealing, dielectric layers and their surface treatment on the nature, density and location of the interface traps and in turn their effects on the performance of the device and its stability are of interest. The completion of the above study is expected to lead to a better understanding of the material system and identification of deposition and other parameters that impact the performance and stability of the TFT devices. This will lead to implementation of these devices successfully on flexible substrates.

2. **Organic/Inorganic Materials Integration**

Another component of this research project was the development of a "hybrid" organic/inorganic LED, or HLED, that integrates inorganic semiconductor and organic semiconductor layers. The purpose of this effort was to create an environmentally stable light-

emitting device. Such a device would reduce the requirements for encapsulation of flexible displays, making them less expensive and more robust. The primary thrusts in this task included device design, development of high work function top electrodes, low work function bottom electrodes, and evaluation of device stability.

Subsequent work will be directed at improving efficiency and stability. Second, we must develop a suitable process for depositing a high work function anode on top of the organic layers (inverted OLEDs, or IOLEDs), and we have made progress in developing a process of IOLEDs. Third, we have investigated techniques for monolayer molecular functionalization of inorganic semiconductors, and have demonstrated preliminary results. Finally, we have evaluated charge injection from inorganic to organic semiconductors and will show preliminary results.

2.1 Summary of Accomplishments

Year 1

- A device architecture for a hybrid LED (HLED) was developed
- Preliminary bottom-injection structures were demonstrated for the cathode layer in an inverted architecture
- Self-assembled monolayer (SAM) treatment of Si cathodes was demonstrated with improved charge injection over untreated substrates

Year 2

- An improved architecture was developed utilizing the bottom-injection structures from Year 1
- Preliminary inverted OLEDs (IOLEDs) were demonstrated with thick anode buffer layers, resulting in functional devices, but large threshold voltage (~14V) and low current efficiency (~0.2 cd/A)
- Improved IOLEDs were demonstrated using a thick, doped anode buffer layer with lower threshold voltage (~9V) but still low efficiency (~0.15 cd/A)
- Further experiments for SAM modification of Si led to optimized treatment conditions
- A study on the effect of plasma pre-treatment on the mechanical properties of transparent conductors demonstrated conditions for improved robustness

Year 3

- Doped buffer layer conditions were optimized to yield improved device performance with a threshold voltage ~5.5V and current efficiency of ~3.1 cd/A. This current efficiency is consistent with the optimum standard OLED
- Stability studies showed that even inverted devices with Al/organic contacts and no low work function component suffer dark spot formation and delamination of the metal contact from the organic layer
- MoO_3 buffer layers were shown to provide further reduced threshold voltage (~4.5 V) but lower efficiency (2.0 cd/A)
- In an attempt to eliminate the use of Ca, H-doping of ZnO was shown to lower the threshold voltage, but only to ~8V
- Deposition conditions for benzoic acid derivative SAMS were optimized

Year 4

- IOLEDs with a thick MoO_3 layer and no organic buffer layer were shown to exhibit significantly improved device stability over previous architectures, but were not stable under continuous operation. Lifetimes exceeding 3 weeks were demonstrated.

Year 5

- IOLED performance was improved to achieve threshold voltage < 6V, efficiency > 2 cd/A, operating lifetimes > 500 hours without encapsulation
- Lifetimes exceeding 1000 hours in ambient storage were observed for other devices with higher operating voltage (~10V)

Year 6

- Further insights were gained into the mechanisms for device degradation and reduced operating voltage, suggesting future paths for simultaneously achieving stable operation and low voltage.

2.2 Summary of Technical Progress

Year 1

The goal of Phase 1 was to demonstrate efficient charge injection and transport using a new electrode structure, and this required outlining a device architecture that could demonstrate the inorganic hybridization principle, while allowing subsequent development into a practical HLED device. First, there must be efficient charge injection and transport into the organic layers. Second, there should be improved stability compared to using low work function metal cathodes. And third, light emission should be demonstrated. We therefore chose a relatively simple device structure using common organic materials, as well as taking advantage of a relatively simple path towards functionalization of the inorganic layers.

The proposed preliminary device structure is shown schematically in Figure 2-1. Key considerations of this design include:

- Use of a Si wafer as a substrate. This was decided primarily for the reasonable electrical properties (work function ~ 4.05 eV) and for convenience while developing a preliminary demonstration device. In addition the transition to a-Si, which may show improved performance due to increased bandgap, or to other wide-gap oxides such as ZnO, is expected to be rather easy. To minimize the work function, n^{++} doped wafers were purchased having □ < 0.004 -cm, and R_s ~40 m□□ sq. One result of this decision is that a transparent top electrode must be used, which is deposited on top of the organic films. The implications of this will be discussed later.

- The use of a BCP hole-blocking layer. We had not previously used this material in our devices, but it was purchased and installed in the system, and process was developed for depositing BCP films. The use of a hole-blocking layer should improve the efficiency of the devices by eliminating hole transport through the Alq_3 film to the cathode. If electron injection from the cathode is relatively inefficient relative to hole injection (which is often the case) this will improve charge balance and restrict recombination to the emitting Alq_3 layer.

- The use of an ITO top anode. ITO films are sputtered on top of the organics, which is a process that can induce excessive damage to the underlying layers. The pentacene film is used as a buffer layer to reduce plasma damage and improve hole injection to the α-NPB layer. This electrode process was evaluated independently, and is still under development, as will be discussed later.
- The use of organic self-assembled monolayers. This is expected to significantly improve the stability between the inorganic layer and the organic layer. In addition, a wide variety of functionalize molecules may be used which could potentially improve the injection characteristics of the cathode. Functionalization of Si surfaces is a highly developed area, which made selection of Si substrates for preliminary devices more logical.

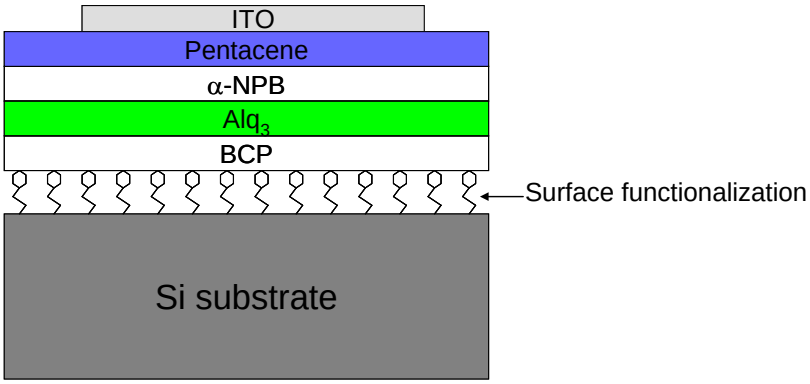


Figure 2-1. Schematic diagram of the preliminary device structure.

i. Development of processes for inverted OLEDs

The development of a process for inverted OLEDs (IOLEDs) is a critical preliminary step to demonstrating HLEDs. This part of the project required a significant amount of effort. The use of an opaque semiconductor as the HLED cathode requires the use of a transparent top anode. The difficulty is that the most common anode material, ITO, must be sputter deposited onto the underlying hole transport layers, and these layers are easily damaged. There have been numerous reports in the literature of developing electrode structures for OLEDs that include a top transparent anode. Some of them include exotic doping schemes that contain reactive metals, which would defeat the purpose of developing more stable cathodes. Other methods use organic layers between the α-NPB layer and the ITO layer to act as a buffer layer, absorbing plasma damage while still effectively transporting charge. Based on the available literature, two materials that appeared to be effective as a buffer layer were CuPc and pentacene. CuPc was investigated first because it was already in our deposition system, and a deposition process was in place.

We initially evaluated electron-only devices, which performed very well. The i-V curves had power-law behavior, with similar current from both electrodes. Sample data are shown below in Figure 2-2.

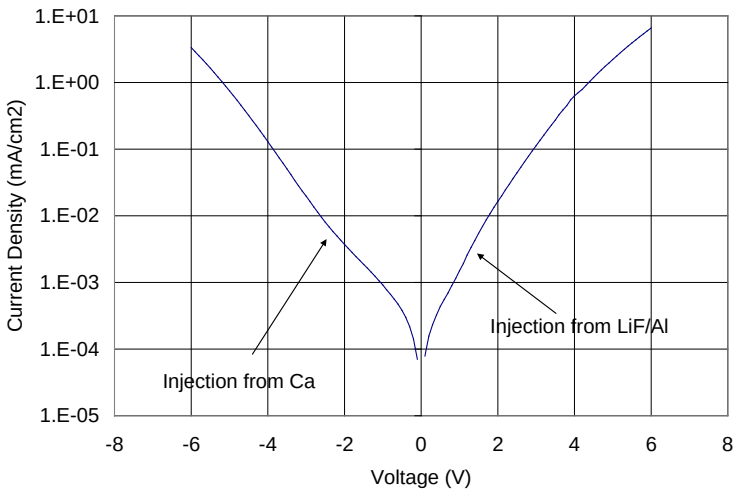


Figure 2-2. Current-voltage characteristics of electron-only device with the structure: Glass substrate/Ti (15nm)/Ag (35nm)/Ca(10nm)/Alq_3(60nm)/LiF(0.8nm)/Al(50nm).

Hole-only devices using a CuPc buffer layer were all shorted, indicating the hole transport/top electrode as the problem. After several approaches to improving the morphology and stability of the CuPc layer, we evaluated pentacene as a buffer layer. Pentacene was reported to be a more effective buffer layer material than CuPc. Unlike the other OLED materials, pentacene is a semiconductor that crystallizes when deposited at room temperature and has a high hole-mobility. However because it crystallizes the films do not have the characteristically smooth morphology of most OLED films. Nevertheless, a process was developed for pentacene deposition for use as an IOLED buffer layer. These efforts also led to films that were highly crystalline with a morphology that did not prevent shorting of the devices. AFM images of the pentacene layer were measured, and are shown below in Figure 2-3. The grain structure is evident, and the Z-range of the image is well above the 30 nm thickness measured by a quartz crystal monitor. These results indicated that pentacene deposited at room temperature was not be a sufficient buffer layer for ITO deposition.

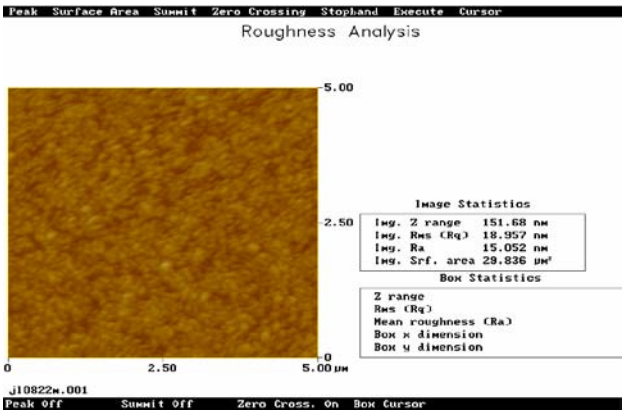


Figure 2-3. AFM image of a 300Å pentacene film.

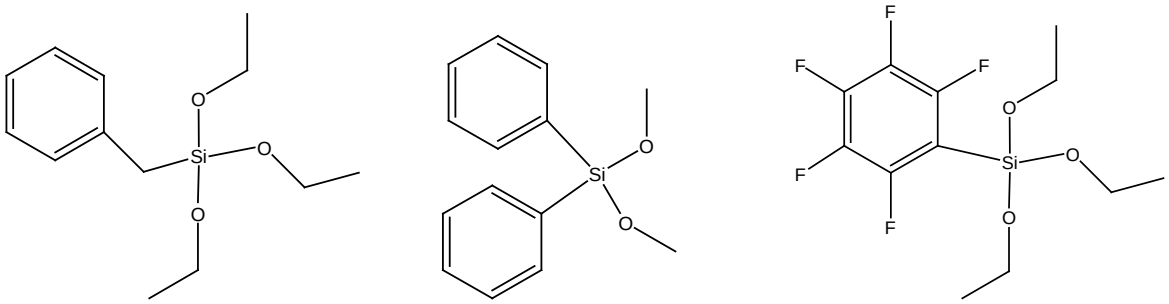
Future plans included the evaluation of a semi-transparent metal, or the use of a semi-transparent metal as a buffer layer for ITO deposition.

ii. Surface modification of c-Si

A critical aspect of achieving efficient injection, and particularly critical for environmental stability, is surface treatments of the inorganic surface. A promising approach is the modification of the inorganic surface with a self-assembled monolayer (SAM). RTI invention disclosures were filed regarding this concept. Much of the literature regarding SAMs deals with thiol-coupling to Au surfaces. However, high work function Au surfaces are not useful as an efficient cathode. Another common application is modification of oxidized Si surfaces. Modification of other types of semiconductors such as III-V compounds has been demonstrated, but the processes are not as well developed. Therefore the selection of Si as a substrate for preliminary demonstrations made sense, with plans to transition the technology to wide-gap semiconductors as the technology is developed further.

There are several considerations when selecting functionalization chemistry. First, the bonding groups must be suitable. The most commonly used compounds employ a trichlorosilane endgroup, which in the presence of moisture, will couple the silicon to an oxide surface. Another useful chemistry employs a methoxy- or ethoxy-silane endgroup, which couples the silicon to the oxide surface without needing moisture. A second consideration is the chain length. Many SAM chemistries use relatively long alkyl chains (6-14 carbons), which would create an unwanted dielectric layer impeding charge injection. Therefore, unusually short/small molecules are of interest. Finally, the endgroup should encourage charge injection by containing pi-orbital bond groups and/or containing a dipole moment to help draw electrons out of the semiconductor. The following molecules were selected for preliminary tests and purchased from Gelest:

Abbreviation	Name	Boiling point (°C)	Drawing
BTO	Benzyltriethoxysilane	148	a
DPDMO	Diphenyldimethoxysilane	161	b
PFPTO	Pentafluorophenyltriethoxysilane	130	c



(a) (b) (c)

Preliminary efforts to functionalize oxidized silicon surfaces use the following procedure:

- Substrate cleaning: n^{++} doped Si wafers are diced into 15 x 22 mm die. The die is cleaned with in acetone followed by isopropanol using ultrasonic agitation and rinsed in DI water. Organic residue is removed by 20 min exposure in a UV ozone cleaner. Finally, inorganic contaminants are removed by a piranha clean. The cleaned die is stored under N_2in a glove box.
- Several mL of reagent is dispensed into 12.5mm diameter x 12.5 mm height quartz crucible in N_2 ambient using a dropper. The crucible is placed inside a 45 mL straight-sided glass jar, and sample is placed alongside the crucible and sealed using a cap with a rubber liner.
- The jar is removed from the glove box and placed inside an N_2 purged oven and heated for a specified time/period.

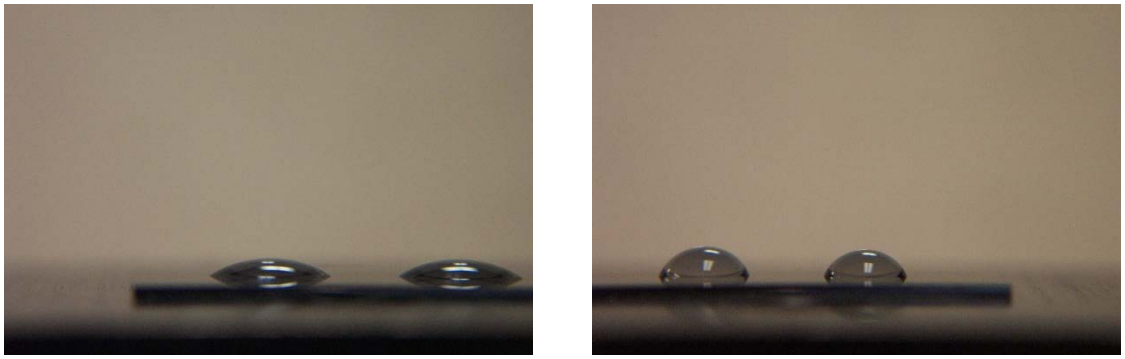
Conditions for time/temperature under reagent exposure so far have ranged from 100 – 130 °C, with a time from 5 – 8 hours. Multiple sample jars can be placed in the oven simultaneously without cross-contamination, and the jars may be re-used.

Spectral ellipsometry can be used to measure the thickness of very thin films, down to several angstroms, provided optical constants of the materials are known. Results for ellipsometric measurements of the first samples using estimated material constants were as follows:

	Oxide thickness (Å)	SAM thickness (Å)	Error parameter
Piranha cleaned Si	22.8	-	1.50
BTO	22.8 (fixed)	0	4.84
DPDMO	22.8 (fixed)	0	1.63
PFPTO	22.8 (fixed)	2.67	1.47

The results indicate that the PFPTO sample has a film present. Because of the zero film thickness and good quality of the fit, the DPDMO likely has no film present at all. The BTO is less clear, but likely has some film present. It is possible that the optical parameters (two different materials were used) were not appropriate, so the lowest error results in a zero film thickness, but better optical parameters would indicate the presence of a film. Further investigation is needed. Attempts to detect the presence of the films using Fourier-transform infrared spectroscopy (FTIR) were unsuccessful.

Contact angle is an extremely surface-sensitive measurement, and therefore very valuable in detecting the presence of surface modifiers. It is a purely "blind" measurement in terms of identifying the surface chemistry, but is very sensitive to changes in surface energy. We used a manual set-up to measure contact angle. De-ionized water was dispensed from a syringe in 15 μl drops, and several drops were dispensed for each sample. A digital camera with a close-up lens was used to capture images, and image processing software was used to measure the contact angle. Both sides of each drop were used, and the values were averaged. Figure 2-4 below shows some sample images of contact angle measurements, and the results are summarized in Figure 2-5.



(a) (b)

Figure 2-4. Images used to measure contact angle for (a) piranha-cleaned Si and (b) PFPTO-treated Si.

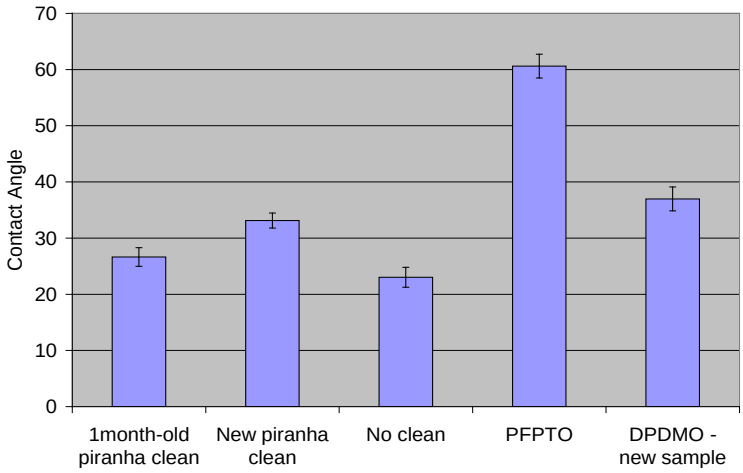


Figure 2-5. Contact angle for various clean and surface treatments for c-Si wafers.

The data in Figure 2-5 show that there is an impact from storing samples for too long, since the aged samples lie in between the fresh and the uncleaned samples. The PFPTO sample clearly has lower surface energy than the untreated sample, and it looks likely that the DPDMO sample has a surface layer, though it is less clear. The fluorinated surface of PFPTO is expected to have the lowest surface energy, so even for equivalent coverage, the effect should be more

pronounced for PFPTO. The BTO samples were tested separately, and all contact angles were offset from this set, and so cannot be compared. These tests should be repeated. We are considering purchasing a commercial contact angle measurement system to improve the accuracy and repeatability of these measurements.

iii. Charge injection from inorganic to organic materials

Electron-only devices (devices with two low work function electrodes and only electron transport layers) can be used to evaluate the charge injection characteristics of electrodes. Electron-only devices were used to evaluate charge injection from c-Si as well as surface-modified c-Si into an Alq_3 electron transport layer. The device structure was: Si wafer/surface modification (if present)/Alq_3 (600Å)/LiF (8Å)/Al (1000Å). This structure allows the comparison of the benchmark cathode for OLEDs (Al-LiF-Alq_3) with the novel c-Si – Alq_3 in terms of injection character.

The results show very unusual behavior that is still being investigated. However in summary, *large currents were possible to achieve injecting from a c-Si cathode*, and therefore the results are very encouraging. Figure 2-6 below shows the i-V characteristics of an electron-only device with c-Si treated with PFPTO. The data show ~2mA current at both +5V and -5V bias. The dot size is 0.05 cm^2, so this is current density is comparable to that expected for OLED devices. More important, *the current density is as good from c-Si as from LiF/Al*, which is the benchmark cathode for OLEDs.

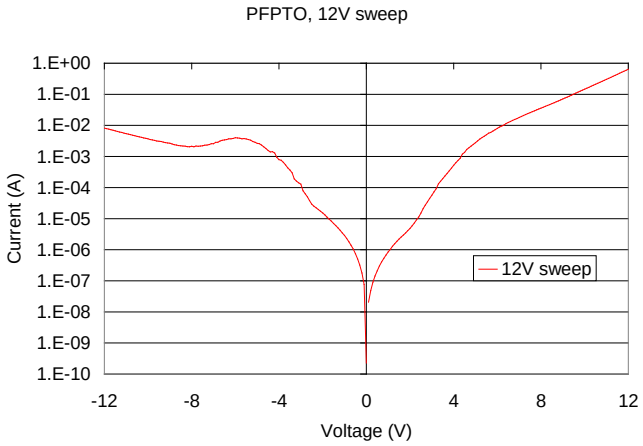


Figure 2-6. Current-voltage behavior for electron-only device with PFPTO-treated c-Si cathode (negative bias) and LiF/Al cathode (positive bias).

Because this behavior appeared to be possibly caused by charge trapping, it was investigated in more detail by observing the current as a function of prior sweeps, which can be used to "reset" trapped charge. For example, after sweeping to 8V (above the anomalous behavior), the voltage was swept to just 4V, then the 4V sweep was repeated. This is shown in Figure 2-7. It can be seen that the first sweep (negative voltage – blue trace) shows similar behavior as in Figure 2-6. However after sweeping to low bias, the forward current increases at low voltages (~1-2V) by 2 orders of magnitude compared with the data in Figure 2-6. In addition, after sweeping to negative bias again (after having swept to a low positive bias), the negative current also increased at low voltage to a similar value (red trace).

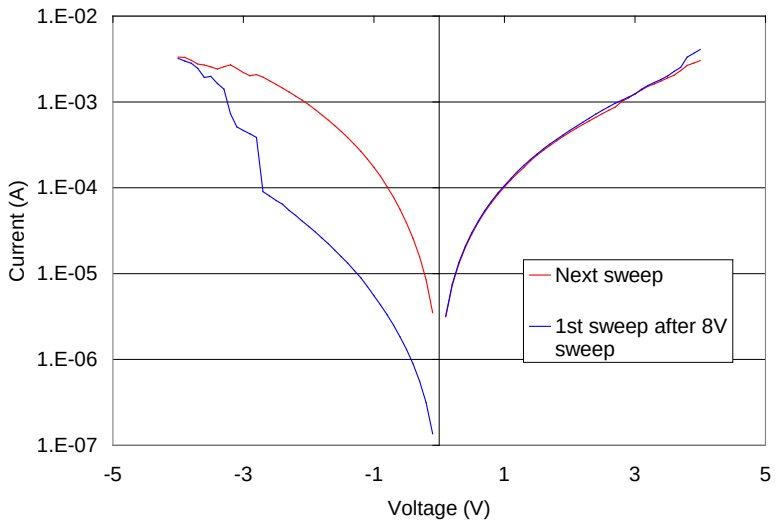


Figure 2-7. DPDMO-treated c-Si sample swept with different bias-histories.

Subsequent sweeps were run, incrementally increasing the voltage above the anomalous feature. Figure 2-8 shows all of the subsequent sweeps, and there are several observations to be made. First, after sweeping to only 4V, the current increased dramatically. Above 4V, the anomalous behavior starts, and with each higher-voltage sweep, the current decreases in the subsequent sweep. This occurs for both polarities. The current jump is more instantaneous for positive bias, and the jump occurs at increasing voltages as the sweep voltage increases.

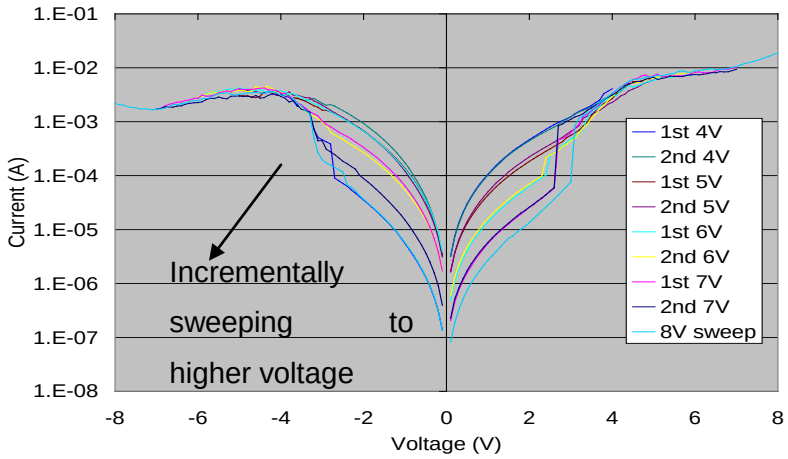


Figure 2-8. Current-voltage sweeps to incrementally higher voltages. The low-voltage current drops after sweeps to higher voltages, and is repeatable.

The interpretation of this behavior was that significant charge trapping occurs in the device, presumably at the c-Si – organic interface, since this is the only novel layer in the device. Because it is repeatable and shows a region of negative differential resistance, it is possible that the trapping and injection is not just trap-to-band, but involves multiple bands. More detailed analysis should be performed to elucidate the mechanisms.

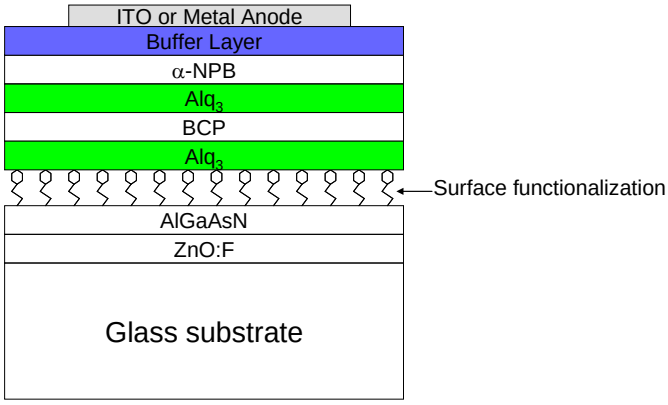
In summary, efficient charge injection has been demonstrated from c-Si and treated c-Si into electron-transport organic layers. This is very encouraging for the development of an efficient HLED device. Anomalous behavior limits the current at higher voltages. This could limit the maximum device current of HLEDs. However when two carriers are present, the field profile through the device changes considerably, and "charge pulling" from opposite carriers could change the injection characteristics. For example, even in traditional OLEDs, it is normally thought that hole injection into the Alq_3 (electron transport) layer enhances injection of electrons into the Alq_3.

Year 2

In Year 2 we suggest some potential improvements to that design. The suggested improvements include:

- Replacing the Si cathode with an ITO/Ca bilayer. In Year 2 this was shown to be an efficient electron injector. With development of inorganic cathodes, this will be replaced with a transparent inorganic/monolayer combination. It also removes the requirement that the top anode be transparent.
- Adding an Alq_3 electron injection layer. We have found that Alq_3 is a more effective electron injection layer than BCP, which can still be used as a hole blocking layer.
- The pentacene/ITO top anode was found to be ineffective, causing too much damage to the organic layers and poor current transport. New buffer layer and top anode structures will be discussed in Section 2.2.

An updated version of the proposed device structure is shown in Figure 2-9.



(b)

Figure 2-9. Preliminary (a) and updated (b) proposed device structure.

i. Development of a top anode structure for IOLEDs

The development of a top anode structure for IOLEDs was the most significant challenge thus far for demonstrating HLED devices. Potential anode materials have characteristically higher melting points than cathode materials, for example Ag and Au (T_m ~ 950 – 1050 °C), or oxide layers deposited by sputtering. These materials damage the underlying organic layers, and can penetrate them, causing shorted devices. Traditional IOLED devices use a buffer layer to prevent damage from the anode, which typically results in higher operating voltage and lower efficiency. A major effort in this project has been the demonstration of a novel top anode structure that overcomes these problems.

Preliminary attempts to sputter deposit ITO onto the organic layers using a pentacene or copper phthalocyanine (CuPc) buffer layer were not effective, resulting in poor rectification and low current densities. Hole-only devices (sandwiching a hole transport material between two high work function electrodes) were shown to be shorted when ITO was deposited, regardless of buffer layer type.

IOLEDs were ultimately demonstrated using a thick CuPc buffer layer (60 nm) and an Al anode, which causes less damage than a comparable Ag anode but requires a high voltage due to the low work function of Al. Figure 2.10 shows the I-V characteristics of a device with the structure: ITO / Ca (20nm) / Alq_3 (60nm) / NPB (40nm) / CuPc (60nm) / Al. Figure 2.11 (a) shows an image of the device with uniform emission, while Figure 2.11 (b) shows the same device with an Ag anode with non-uniform emission indicative of damage. Compared to standard OLED devices, the current efficiency of the IOLED device is ~10x lower, and the threshold voltage is ~14V rather than ~4V.

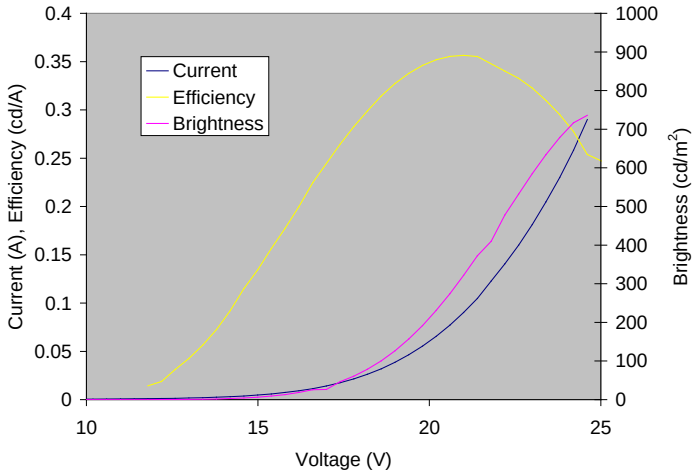
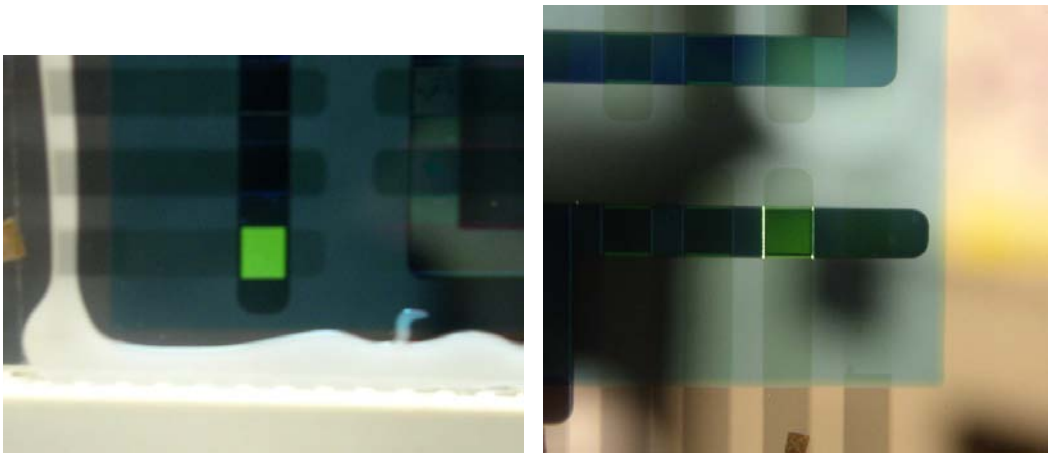


Figure 2-10. IOLED device with a thick CuPc buffer layer and Al anode.



(a) (b)

Figure 2-11. Images of IOLED devices with (a) Al and (b) Ag anodes.

Efforts continued to identify more suitable buffer layers. The first approach was the use of a plasma-deposited, Teflon-like, CF_x polymer layer. Thin CF_x layers are commonly used as an interface modification for traditional bottom anodes, between the ITO and the hole transport layers. It has been proposed that fluorine in the CF_x layer partially dopes the organic layers. It was proposed that a CF_x layer could provide effective protection and optical transparency. CF_x was deposited in our OLED deposition system by plasma polymerization from C_4F_8. The conditions used were 10W RF power, 40 mTorr, 15 sccm C4F8. The low power was intended to minimize damage to the organic layers. Spectroscopic ellipsometry showed that the deposition rate was 1 Å/sec, linear with deposition time. IOLED devices were fabricated using CFx buffer layers. The device structure was: ITO / Ca (10nm) / Alq (60nm) / NPB (40nm) / CuPc (15nm) / CFx (6nm) / Ag or Al (60nm). Despite the effective reduction in shorting by 60Å CFx using Ag top anodes, the full devices using Ag were completely shorted. The devices with Al top anodes were not entirely shorted, but showed signs that the anode metal formed filamentary structures under bias. This is demonstrated in Figure 2.12. The 1st sweep data show a threshold voltage of ~2-3V, which is expected for these devices, but then a rapid and linear increase in current. Subsequent voltage sweeps repeatably show ohmic, low-resistance behavior up to ~2V followed by a decrease in current. This is indicative of the formation and burn-out of metal filaments. At this stage, the pursuit of CF_x buffer layers was suspended.

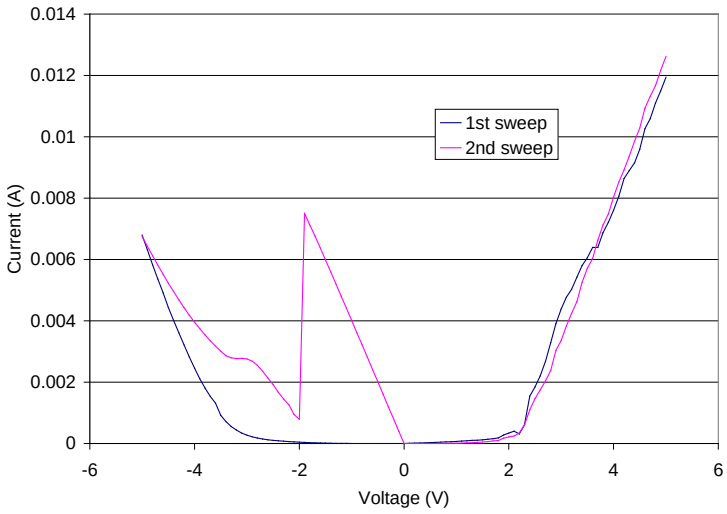


Figure 2.12. I-V data for IOLED device using a CF_x buffer layer and Al top anode.

An alternative approach was the use of Cu_2O as a buffer layer. Cu_2O is a well-known p-type semiconductor, making it a promising buffer layer material, in that it can be deposited with considerable thickness while still providing efficient charge transport. In addition, it is reported to sublime at low temperatures (~500 - 600°C) leading to minimal damage of the organic layers.

Attempts to thermally sublime Cu_2O layers were not successful, as the results did not conform to what was expected from the literature. The next attempt to form Cu_2O buffer layers was reactive sputtering of Cu. Modeling preliminary films with spectral ellipsometry showed that the film was similar to CuO, rather than Cu_2O.

IOLED devices were fabricated and a device with 37.5 nm CuO_x emitted light and was stable at 15V. The subsequent experiment was to fabricate IOLEDs with 37.5 nm CuO_x with varying O_2 concentration in the buffer layer. The I-V results from these devices are shown in Figure 2.13. The O_2 content did not have a strong effect on the devices, but current increased with decreasing O_2. Compared to devices using thick CuPc as the buffer layer the CuO_x devices turn on at much lower voltage but have a very gradual turn-on behavior. This indicates that the CuO_x energy levels are favorably aligned with CuPc for low-voltage injection, but the high resistance prevents sufficient current flow. Without a clear path to increasing the current flow CuO_x films were abandoned as buffer layers for IOLEDs.

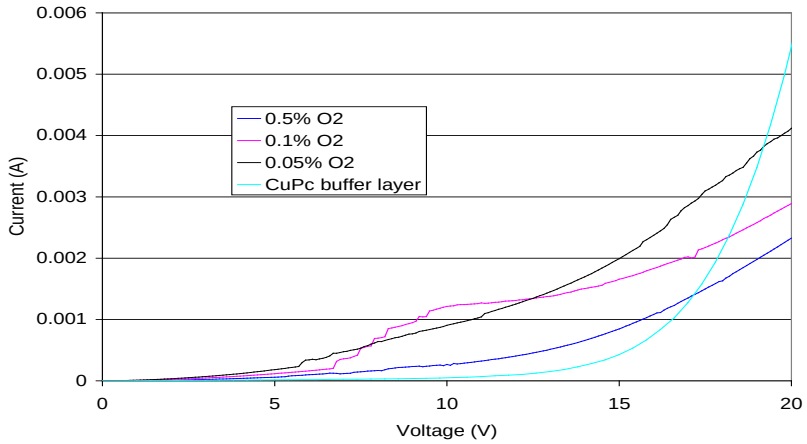


Figure 2-3. I-V behavior of IOLEDs with different O_2 concentrations in the sputter gas while depositing the CuO_x buffer layer. The device with thick CuPc is shown for reference.

Another reported method for achieving high efficiency, low-voltage IOLEDs in the literature is to utilize relatively high conductivity doped injection layers with undoped recombination layers, resulting in a PIN configuration. By using a thick, doped buffer layer, anode damage is prevented without a substantial increase in threshold voltage. Figure 2-14 shows the device structure and Figure 2-4 shows the i-V characteristics for a device with the structure: ITO / Ca (25nm) / Alq_3 (60nm) / NPB (40nm) / m-MTDATA:F4TCNQ(2%) (100nm) / Al or Ag. The device with the Ag electrode results in higher leakage current, but also in lower operating voltage. The Al devices show a low threshold voltage – just ~3V – but a very slow slope, leading to higher operating voltage than desired. Interestingly, the emission spectrum of these devices is unlike the standard NPB/Alq_3 bilayer structure. Figure 2.16 shows the emission spectra for device with Al and Ag anodes. The blue component is likely to result from emission in either the NPB or the m-MTDATA layer. The orange component is likely to result from F4TCNQ emission. It follows that the Ag device would have a smaller orange component, as the Ag is likely to penetrate further into the buffer layer. It was also observed that there is a very strong interference effect – emission color changes strongly with angle. Further experiments were needed to optimize the structure to achieve emission and recombination in the desired recombination zone.

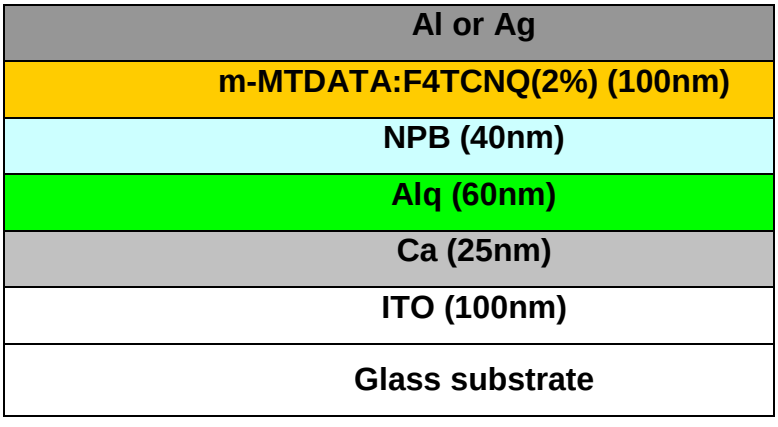


Figure 2-14. Schematic diagram of the Year 2 IOLED.

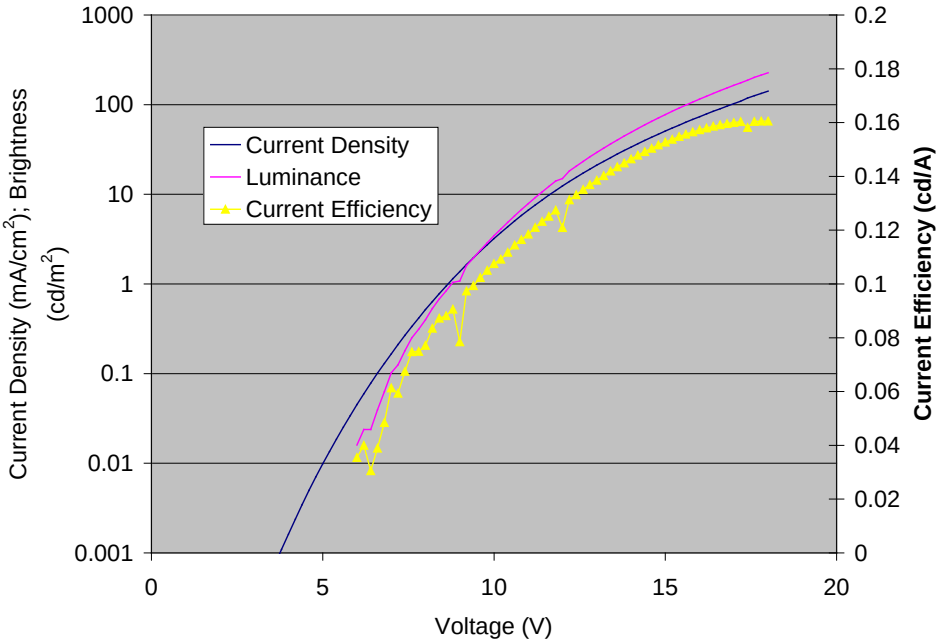


Figure 2-4. L-I-V and efficiency data for preliminary IOLED devices with an organic buffer layer.

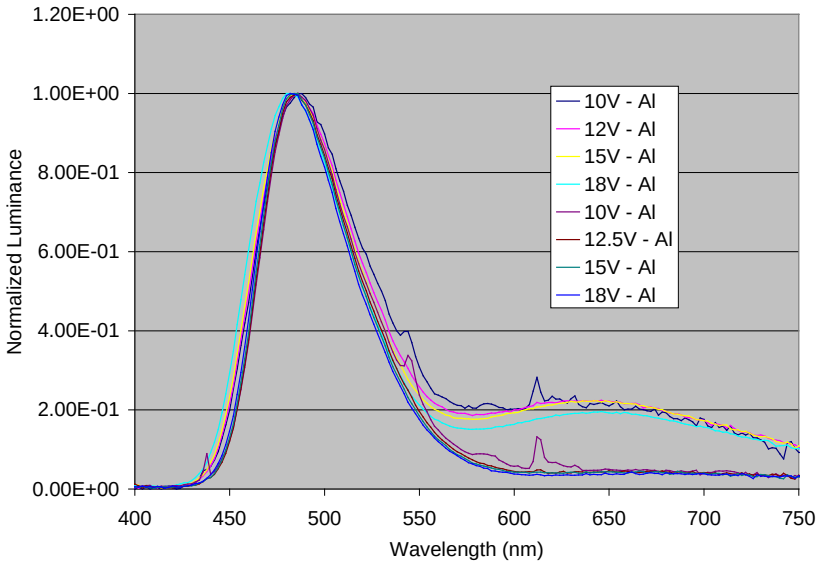


Figure 2-5. Emission spectra for IOLED devices at different threshold voltages.

ii. Molecular Functionalization of Inorganic Semiconductors

In Year 1 we had demonstrated a method for gas-phase formation of self-assembled monolayers (SAMs) on Si. Preliminary experiments in Year 1 showed that SAMs were formed from PFPTO, but not from BTO or DPDMO from the gas phase process. In Year 2, **Kellen Gibson from NC A&T** developed a more detailed procedure for the formation and characterization of SAMs on Si substrates.

Solution processing showed superior results over vapor phase deposition, so this method was used most frequently. The substrates for SAM formation were n^+ Si. The films were primarily characterized using contact angle goniometry, which indicates a change in surface energy, and is highly sensitive to surface chemistry. Ellipsometry was also used, and XPS was used to characterize select samples.

iii. PFPTO Contact Angle Results

Figure 2.17 shows the contact angle of PFPTO SAMs as a function of time for different temperatures. The concentration of the PFPTO solution (0.5 mM and 5 mM) did not affect contact angle. Control samples varied from 15° to 30° and therefore are denoted by the dashed lines. The results showed that very long deposition times were required for room temperature processing, but just 60 minutes at 50°C was sufficient to increase the contact angle, and the saturation with time indicates that this is the value indicating full coverage. Samples processed at 70°C, regardless of time, resulted in low contact angles, indicating that organic residue was left on the surface. These results indicate that deposition temperature is the most critical parameter for PFPTO SAM formation.

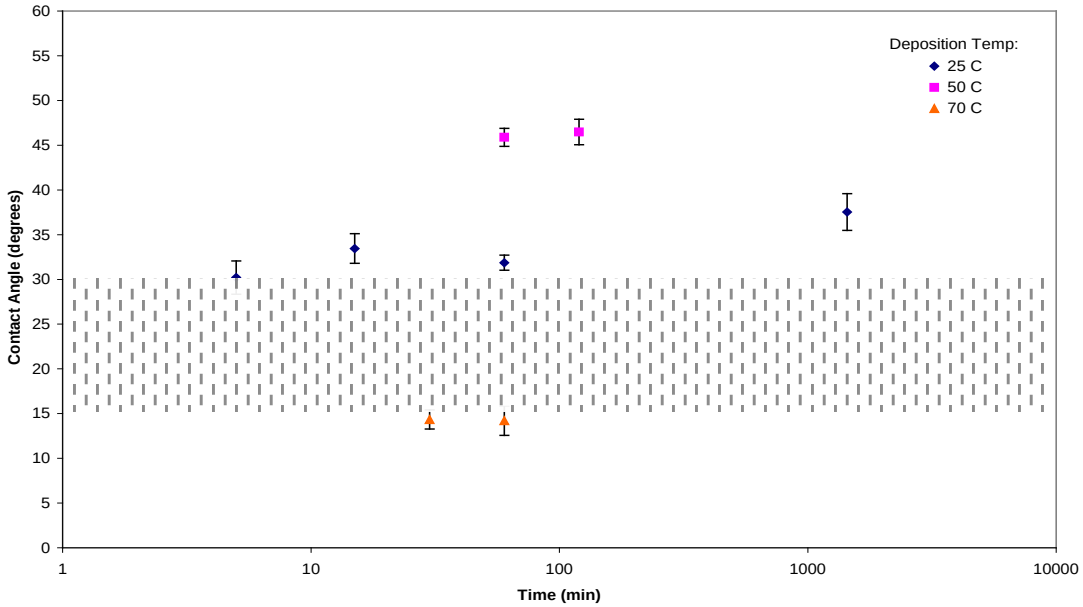


Figure 2-6. Pentafluorophenyltriethoxysilane (PFPTO) contact angle as a function of immersion time at temperatures of (◆) 25 °C, (■) 50 °C, and (▲) 70 °C.

iv. BTO Contact Angle Results

Figure 2.18 shows contact angle results for BTO at various temperatures as a function of time. The concentration for BTO precursors in these samples was 1 mM. All samples dipped for less than 120 minutes were within the boundaries of the control sample conditions, but as the temperature and dipped time increased, contact angle or surface coverage also increased. The maximum contact angle is observed at a dip time of 240 minutes, so it is not clear that a saturated layer has been achieved. When increasing the temperature to 70 °C, the contact angle also increases, but is comparably smaller than the samples dipped at 50 °C. The general trend of higher contact angle with time for all temperatures indicates that BTO layer formation has a lower thermal activation energy, but is more strongly dependent on time.

v. DPDMO Contact Angle Results

DPDMO at 1mM for various times and temperatures is demonstrated in Figure 2.19. Samples dipped in DPDMO did not display any significant shift in contact angle with dipping duration and temperature, indicating that either (a) the conditions used were not favorable for monolayer formation or (b) that the surface energy of a DPDMO surface is comparable to toluene-treated Si. Given the similar chemical nature of DPDMO with BTO, it seems more likely that a monolayer was not formed.

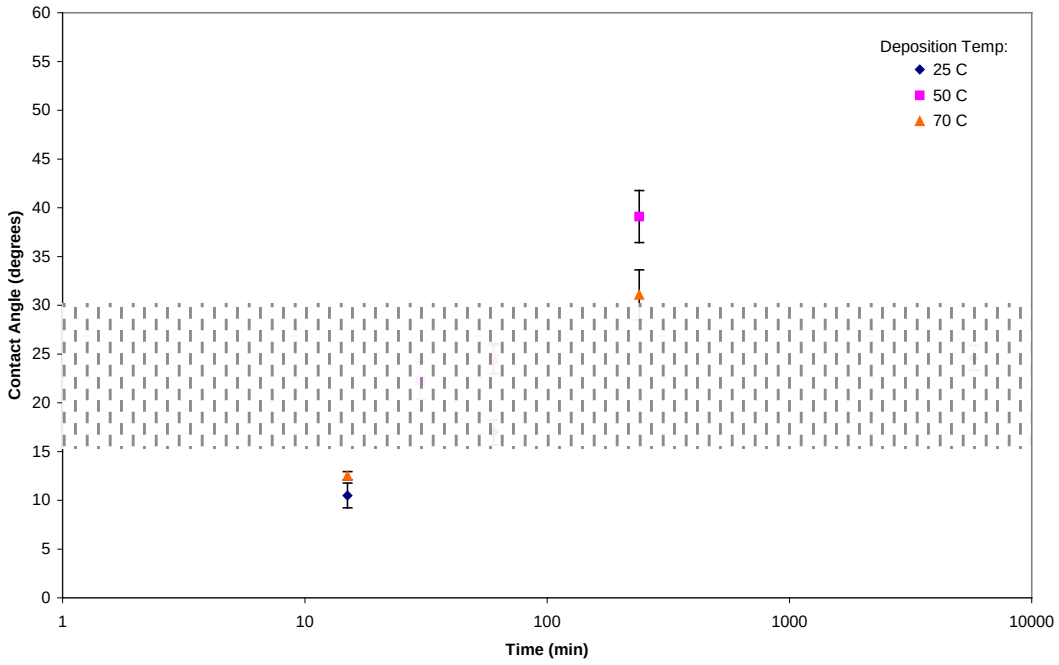


Figure 2-18. Benzyltriethoxysilane (BTO) contact angle vs. immersion time at temperatures of (◆) 25 °C, (■) 50 °C, and (▲) 70 °C.

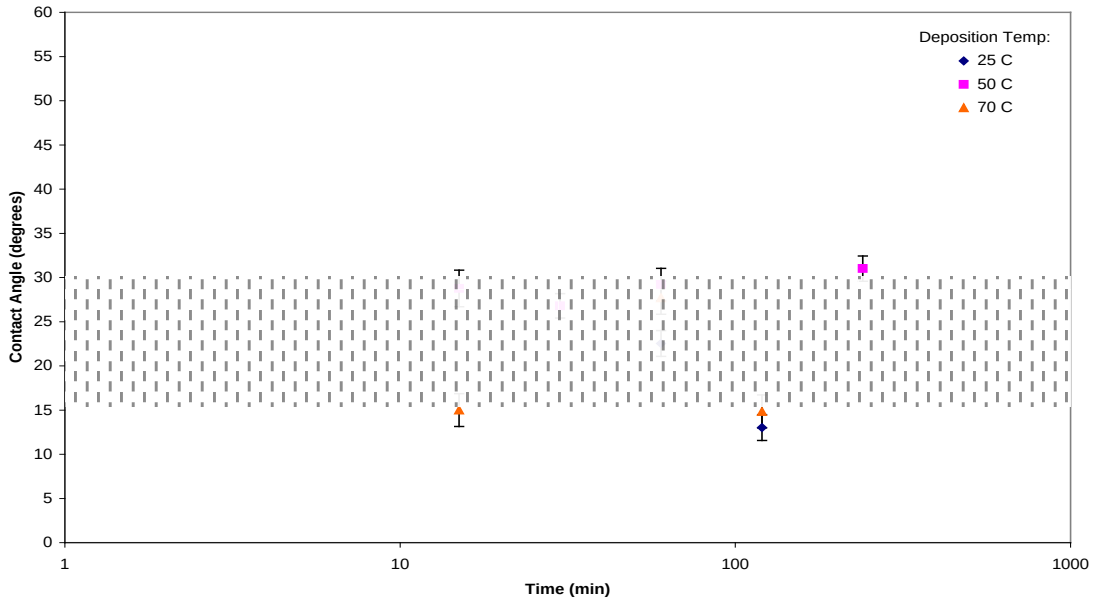


Figure 2-7. Diphenyldimethoxysilane (DPDMO) contact angle vs. immersion time at temperatures of (◆) 25 °C, (■) 50 °C, and (▲) 70 °C.

By the end of Phase 2 the SAM formation process was completely transferred to Professor **Iyer's** labs at NC A&T.

In addition to the top transparent anode, another requirement is an efficient charge injection mechanism from a transparent conductor into the inorganic semiconductor. Transparent conducting oxides (TCOs) are routinely used in OLED devices, typically with indium-doped tin oxide (ITO) as a transparent anode. The work function of ~4.5 eV for ITO can be modified to values in the 3.9 – 5.1 eV range using a variety of techniques, which makes it more suitable as a hole-injecting electrode. A tremendous amount of work has been done to optimize the ITO-organic interface to optimize charge injection, and this interface is generally considered very stable. However due to their typically large work functions, TCOs have not been pursued as a solution for electron injection, where they could provide the same benefits to the problematic cathode-organic interface.

Work functions for typical and some novel TCOs are included in Table 2-I. From this list, it is apparent that ZnO is the most promising candidate for a low work function electrode. Still, the value of 4.5 eV is too large for efficient charge injection in Alq_3-based OLEDs. Doping ZnO with F to achieve higher conductivity also results in a reduced work function of 4.2 eV, similar to the effect that F-doping has on SnO_2. If F-doping is optimized in the ZnO system for low work function, rather than maximum conductivity, it is likely that the work function may be reduced further simply by optimizing dopant concentration, stoichiometry, and processing conditions. Based on these observations, we chose to investigate the use of ZnO:F as a low work function TCO for HLED devices, either as an injection layer into the III-V transport layer, or even as a direct injection layer.

Table2-1. Work function (ϕ) of some common metals used in OLEDs and transparent conductive oxides.

Compound	**ϕ (eV)**
Li	2.9
Ca	2.9
Mg	3.7
Al	~4.1
ZnO:F	4.2
ZnO	4.5
ZnO:Al	4.6
ITO	4.4-4.8
SnO_2:F	4.4-4.9
SnO_2	4.8
In_2O_3	4.7
$ZnSnO_3$	5.3
$GaInO_3$	5.4
$MgIn_2O_4$	4.8

vi. Mechanical Evaluation of Transparent Conductors for Environmentally Stable Flexible Displays

Another component of the project is the investigation of mechanical limitations of brittle films used in flexible display applications. NC A&T and RTI collaborated on this effort with Professor **Terry Alford** from Arizona State University and the U.S. Army Flexible Display Center.

Indium-tin-oxide thin films were deposited on PEN polymer substrates using rf sputtering at substrate temperature (T_s) of room temperature and 100 °C. Before being introduced into the chamber, we did substrate plasma pre-treatment at three different plasma gas such as Ar, O_2, and N_2H_2. The sputtering target used in this experiment was In_2O_3 containing 10 Wt% SnO_2. The constant distance of substrate to target was 6 cm and maintained for all the deposition. The base pressure before deposition was about below 1×10^{-7} Torr and working pressure is about 8 mm Torr. The sputtering was conducted in the mixture of Ar – O_2 atmosphere. The oxygen gas ratio was 0.05% and gas flow rate was 100 sccm. ITO samples were deposited at different rf power of 60 and 120 W. Silicon (Si) wafer substrates were placed in equidistance position with PEN substrate to obtain simultaneous ITO deposition on both substrate to determine thickness by using ellipsometry.

This films were evaluated using X-ray diffraction analysis (XRD) and Hall effect measurements to measure carrier concentration, Hall mobility, and resistivity by means of the van der Pauw method. Table 2.2 summarizes the processing conditions for each sample as well as the sheet resistance, Rs, on a monitor Si substrate as well as on PEN, the % increase for Rs on PEN vs. Si, the average optical transmission in the 450 – 650 nm wavelength range, and the thickness.

Table 2-2. Summary of processing conditions and sheet resistance / transmission results for the ITO bending study.

Sample	Plasma gas	Power	Dep Temp	Dep Time	Rs (Si)	Rs (PEN)	% increase	Avg transmission	Thickness
944	Ar	60	30	526	29.5	31.5	7.1	82.6	*1371*
945	O2	60	30	526	37.8	49.7	31.6	86.4	*1261*
946	N2/H2	60	30	526	33.2	40.9	23.3	81.9	*1143*
948	N2/H2	120	30	237	61.2	82.3	34.6	70.7	*1409*
949	O2	120	30	237	90.7	168.6	85.9	85.5	*1302*
950	Ar	120	30	237	47.3	68.6	45.1	74.6	*1360*
951	N2/H2	60	30	526	19.6	50.0	155.2	77.8	*1459*
953	Ar	60	100	526	31.9	30.8	-3.4	80.4	*1474.0*
954	O2	60	100	526	28.0	29.15	4.1	82.2	*1331.0*
956	N2/H2	60	100	526	27.4	28.3	3.3	81.7	*1279.0*
957	N2/H2	120	100	237	19.7	16.1	-18.3	83.2	*1463.0*
958	Ar	120	100	237	18.3	18.4	0.5	82.6	*1456.0*
959	O2	120	100	237	15.6	15.35	-1.6	83	*1534.0*
961	Ar	60	100	526	26.7	29.7	11.2	82.2	*1283.0*

Hall measurement results and oxygen content from RBS measurements are shown in Table 2.3.

Table2-3. Four-point probe, Hall measurement, and O_2 concentration from RBS measurement results for the ITO samples in this study.

Sample	Rs (from RTI)	Resistivity (Ω-cm)	Mobility (cm^2/Vs)	Carrier concentration (/cm^3)	Oxygen content (atoms/cm^2)
944	31.5	4.60×10-4	30.2	4.49E+20	4.93E+18
945	49.7	7.20 × 10-4	27	3.28E+20	4.77E+18
946	40.9	4.40 × 10-4	40	3.50E+20	4.77E+18
948	82.3	8.57 × 10-4	12.7	5.80E+20	4.83E+18
949	168.6	2.40 × 10-3	22	1.18E+20	4.83E+18
950	68.6	9.02 × 10-4	11	6.28E+20	4.78E+18
951	50	6.95 × 10-4	13	6.70E+20	4.92E+18
953	30.8	3.91×10-4	25.1	6.35E+20	5.19E+18
954	29.15	5.32 × 10-4	29.3	4.01E+20	4.7E+18
956	28.3	4.74 × 10-4	32.4	4.06E+20	4.98E+18
957	16.1	5.32× 10-4	18.1	6.48E+20	4.95E+18
958	18.4	3.6 × 10-4	20.8	8.33E+20	4.9E+18
959	15.35	2.09 × 10-4	25.4	1.18E+21	5.1E+18
961	29.7	5.13 × 10-4	28.7	4.24E+20	4.86E+18

The samples were tested for failure radius using RTI's x-y-theta bend test apparatus. Table 2.4 summarizes the average critical radius, R_c, which is defined as the radius at which the resistance of the sample doubles, as well as the standard deviation from several measurements.

Table 2-4. Critical radius (Rc) and standard deviation of Rc for the ITO samples in this study.

Sample	Rc	Std Dev.
944	7.87	0.08
945	7.75	0.25
946	7.58	0.33
948	8.86	0.33
949	10.01	0.56
950	10.90	0.99
951	8.96	0.72
953	7.57	0.00
954	7.25	0.30
956	6.86	0.26
957	8.41	0.30
958	8.68	0.36
959	10.30	0.56
961	7.31	0.56

In the subsequent phase we analyzed the preceding data (including other data not shown) to study the influence of process conditions on physical, chemical, and microstructural properties, and to gain an understanding of which properties influence the mechanical robustness of ITO as a transparent conductor for flexible displays. The results were submitted for publication, as noted in the list of publications.

Year 3

In Year 3 it was observed that the Al/organic interface is intrinsically unstable leading to degradation, regardless of the presence of reactive elements such as Li or Ca. Thus we focused on alternative device structures than those developed to date. As demonstrated below, we have recently developed an inverted device structure with an oxide-based hole injection layer. This would prove to be a critical step, and the oxide/organic interface was key to providing a chemically stable interface with efficient charge injection.

Preliminary efforts in Year 3 were to reduce the operating voltage and increase the current efficiency of the device using doped organic layers presented in the previous section from ~0.15 cd/A to ~3-4 cd/A.

i. Doped organic buffer layers

Devices of the type similar to the one measured in Figure 2-4 showed very slow increase in current with voltage, as well as low efficiency. The first area of optimization was in the top anode structure. A relatively thick, doped buffer layer was effective in preventing damage to the device,

but added substantial resistance. We chose two different routes towards improving this layer. The first was to optimize the thickness and doping concentration of the buffer layer.

Table 2-*5* summarizes the results of this study. Although Ag has a higher work function, it does not appear to be compatible with a doped organic buffer layer. When the thickness is optimized for lower voltage operation, stability is compromised. Aluminum works reasonably well, though the threshold voltage is fairly high and the current-voltage slope is still rather low. The performance is not highly dependent on doping concentration. Device OL-1039c gave the best performance, and was a good place to start in terms of replacing the cathode with stable inorganic materials.

Table 2-5. Summary of doped organic buffer layer study.

Run#	m-MTDATA: F4TCNQ layer thickness (Å)	F4TCNQ doping concentration (wt%)	Anode metal	Comments
OL-1036a	800	2	Al	η~2.5cd/A, 1mA@9.6V, orange
OL-1036b	500	2	Al	η~1.75cd/A, 1mA@9.8V, orange-green
OL-1036c	300	2	Al	Noisier, η~2.75cd/A, 1mA@9.0V, green emission (no angular effects
OL-1036d	800	4	Al	Similar to (a), eff~3.0, 1mA@9.6V, 100cd@11.4V
OL-1038a	300	4	Ag	Green, eff~2.1@10V, 100cd@7.9V, 1mA@7.5V, but not stable – gets hot spots and burns out
OL-1038b	500	4	Ag	Unstable
OL-1038c	300	8	Ag	Unstable
OL-1038d	500	8	Ag	Unstable
OL-1039a	300	4	Al	150ÅCa; similar to 1039c, but slightly less stable
OL-1039b	300	8	Al	150ÅCa; splotchy appearance at lowV, otherwise similar
OL-1039c	300	4	Al	50ÅCa; **Best doped organic buffer device**; η~3.1cd/A, 1mA@8.2V, 1nit@5.5V, 100nit@8.2V, , green, no angular dependence, stable to 19V
OL-1039d	300	8	Al	50ÅCa; almost same as 1039c but slightly higher voltage

ii. Oxide-based buffer layers

An alternative to organic doped layers is the use of a p-type inorganic semiconductor with a low vaporization/sublimation temperature. In Year 2 we evaluated the use of CuO_x for such a material. In Year 3 we investigated the use of MoO_3 as a buffer layer material, both as a pure oxide and as a dopant in m-MTDATA. Both have been shown to be effective as injection layers for standard OLEDs, where the oxide/doped layer is deposited on ITO, prior to organic layer deposition. Devices using the structure shown in

Figure 2-20 were evaluated.

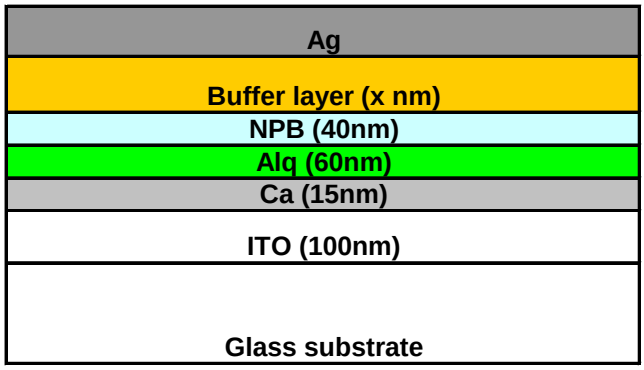


Figure 2-20. Device structure for IOLEDs using oxide or oxide-doped buffer layers.

In preliminary devices the buffer layer consisted of pure MoO_3 and showed anomalous behavior. The devices typically began an i-V with a nearly ohmic behavior, referred to as a "dc-short," then current decreases and the devices exhibit typical space charge-limited behavior. This behavior is repeatable when re-tested a given device. A typical set of I-V curves from a device with 5nm MoO_3 and an Ag anode is shown in

Figure 2-21.

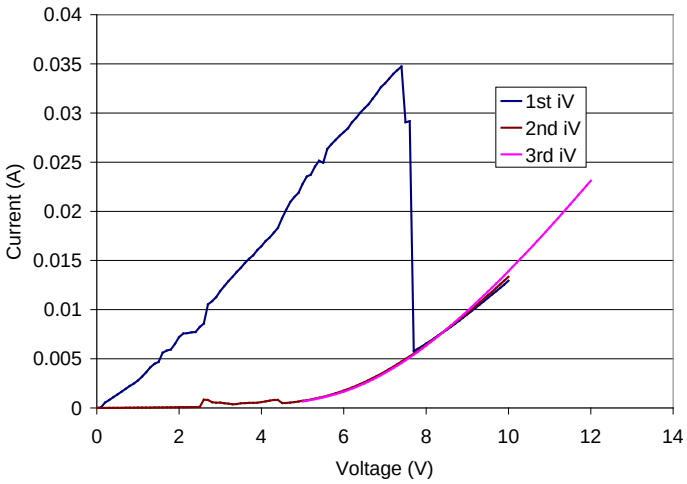


Figure 2-21. Current-voltage behavior typical of devices with a pure MoO_3 buffer layer.

The reason for the interest in this behavior lies in the resulting device performance. This is demonstrated in Figure 2-22 and Table 2-6. The operating voltage for MoO_3 buffer layer inverted devices is much lower than for doped organic buffer layers, and approaching that of optimized standard OLEDs. The efficiency of ~2 cd/A is lower than the 3.5 cd/A target for standard devices, but this is not surprising considering that the layers were not optimized for this devices structure. At this level of performance, it is not clear whether a larger improvement would come from optimizing the bottom Ca/Alq_3 interface or the top anode interface. The goal becomes achieving the performance of MoO_3 injection layers, but without the aberrant "dc-shorting" behavior, and

with improved stability. At this stage, however, the top anode performance was deemed sufficient to begin focusing on the development of inorganic, stable, bottom cathode layers.

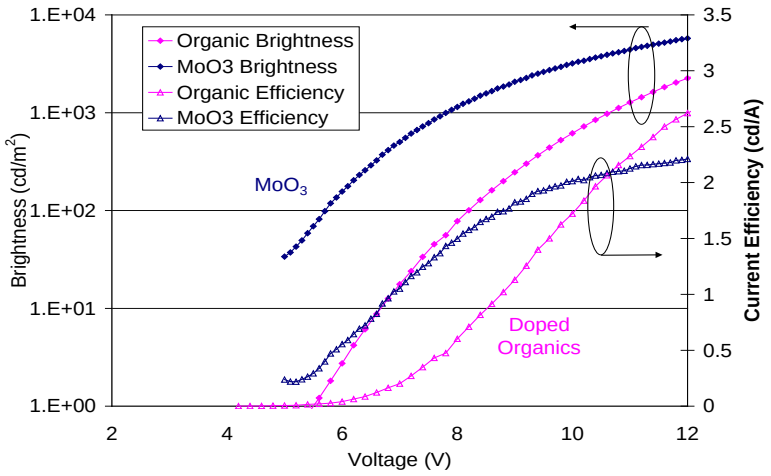


Figure 2-22. Comparison of B-V and η-V curves for MoO_3 buffer layers vs. doped organic (m-MTDATA:F4TCNQ) buffer layers.

Table 2-6. Summary of Doped organic vs. MoO_3 buffer layer vs. standard OLED performance metrics.

	OL-1039C	OL-1048A	
Brightness	Doped organic	MoO_3	Std OLED
1 cd/m^2	5.5V	4.0	3.1
100 cd/m^2	8.2	6.1	5.3
1000 cd/m^2	10.6	8.2	7.5

iii. Bottom cathode layers

It was outlined previously that ZnO based materials were the most promising among transparent conducting oxides for achieving a low work function, efficient cathode. Specifically, ZnO:F was targeted for the best performance. For baseline device studies, however, pure ZnO was used, with doping to be considered for subsequent optimization. It was also reported that subjecting ZnO to H_2 plasma would effectively dope and lower the work function of ZnO. In addition, it has been reported that acid/base treatments of ITO can effectively modify the surface to result in a surface dipole, effectively modifying the work function. We evaluated the charge injection performance of these modified ZnO films into Alq_3 by fabricating "electron-only" devices, and comparing the bottom electrode injection to the standard LiF:Al top cathode. The device structure is shown in Figure 2-.

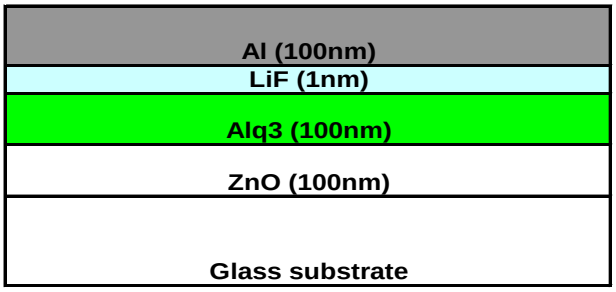


Figure 2-23. "Electron-only" device structure used to evaluate cathode performance relative to a baseline LiF:Al cathode.

Two standard cathode treatments were used. The first was dipping the ZnO film into tetrabutylammonium hydroxide ($N(C_4H_9)_4OH$) solution, which is reported to have the largest effect of lowering the work function of ITO. The second treatment was H_2 plasma, performed using 90% N_2 / 10% H_2 at 40 mTorr in a planar RF diode configuration. A summary of the results is given in Table 2-7. In general, better charge injection is achieved when the current at 10 V bias is larger, or when the voltage required for 1 mA current is lower. The base-treated samples typically resulted in a preliminary I-V sweep with very high currents, followed lower currents for subsequent sweeps. This was interpreted to indicate that a surface dipole does, in fact, provide increased charge injection, but that the OH-based dipoles are not stable under high electric fields. The H_2 plasma resulted in increasingly poor performance at 10W RF power. However the best results for stable, electron-only devices came from a 40 minute plasma exposure at 6W RF power. This treatment was used for subsequent inverted HLED experiments.

Table 2-7. Performance of electron-only devices with different surface treatments.

Run#	Treatment	I at 10V	I at -10V	V at 1mA	V at -1mA	Comments
1064A	Std ITO	8	0.5			
1065A	ZnO	9	1	4.2	-10	
1068A	1min H2, 10W	3	.2	6	-	
1068B	10min H2, 10W	3	.07	6.8	-	
1068C	60min H2, 10W	3	.03	6.2	-	
1069A	20min H2, 6W (A)	3	.3	6.6	-	
1069B	10mM,20min (B)	6	.15	6.4	-	
1069C	(A)+(B)	8	1	5.4	-10	
1070A	1 min, 1mM	.9	5.5	5.5	-10	
1070B	5 min, 1mM	1.5	5.4	5.4	-9.4	
1070C	20min, 1mM	1	5.2	5.2	-10	
1065D	**40min H2, 6W(C)**	**1.5**	**5**	**6.0**	**-8**	Lowest voltage for 1mA rev. bias current
1071C	40min 10mM(D)	.2	6	5.0	-	
1071D	(C)+(D)	1	5	5.0	-10	
				5.0		

iv. Inverted HLED devices

Preliminary inverted HLED devices were fabricated with the structure shown in Figure 2-8. These devices showed characteristic green emission from Alq_3, but only very weakly and with very poor efficiency ($\eta \sim 10^{-3}$ cd/A, operating voltage ~16-18 V).

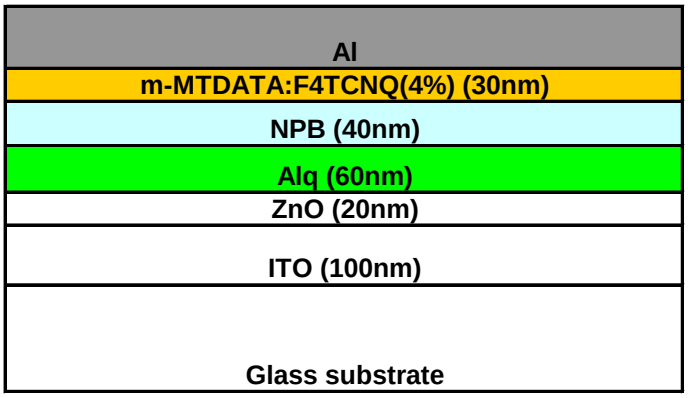


Figure 2-8. Preliminary inverted HLED structure.

The next step forward in improving the HLED devices used structures similar to the one in Figure 22-9. Two significant changes are (a) the inclusion of a BCP hole-blocking layer, and (b) H_2 plasma modification of the ZnO cathode. Traditional Alq_3 – NPB based OLEDs are optimized such that nearly equal amounts of charge are injected by the cathode and anode, respectively. For more complex structures, a hole-blocking layer such as BCP is included. BCP allows injection of electrons, but provides a large barrier to hole transport. This leads to substantial improvements in devices that are electron deficient. The resulting performance of HLEDs is shown in Figure 2-10. There are several points to note. First, initial measurements show *extremely high* efficiency values. Optimized traditional OLEDs based on the same materials typically do not exceed 3.5 cd/A current efficiency, while these devices show a maximum value of ~4.4 cd/A. However, this performance is not stable. After operating for several minutes, the performance decreases to the values shown in Fig. 2.21 labelled "3rd sweep" which is still very high. However, the operating voltage is substantially higher than standard devices. The anode structure in this device is identical to the device whose performance is summarized in Table 2-6. Summary of Doped organic vs. MoO3 buffer layer vs. standard OLED performance metrics.Table 2-6, labeled "doped organic" buffer layer. In comparison, the HLED device operating voltage is higher, which is therefore attributed to the cathode structure. Therefore improved cathode performance is needed, as outlined later. Overall, the performance is quite good, and represents the first device of its kind. Moreover, clear methods to improve the performance are known, also outlined later.

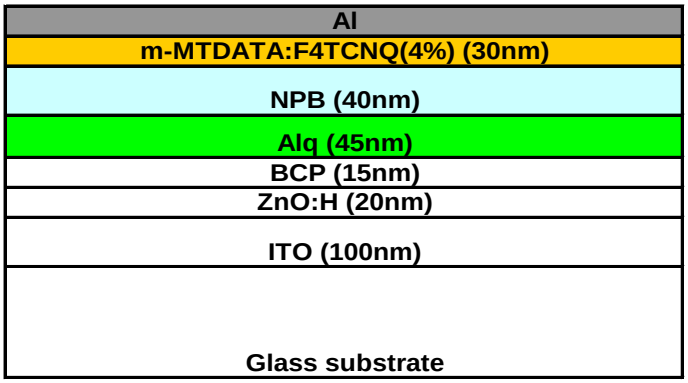


Figure 22-9. HLED device structure using a BCP hole blocking layer and H_2 modified ZnO cathode.

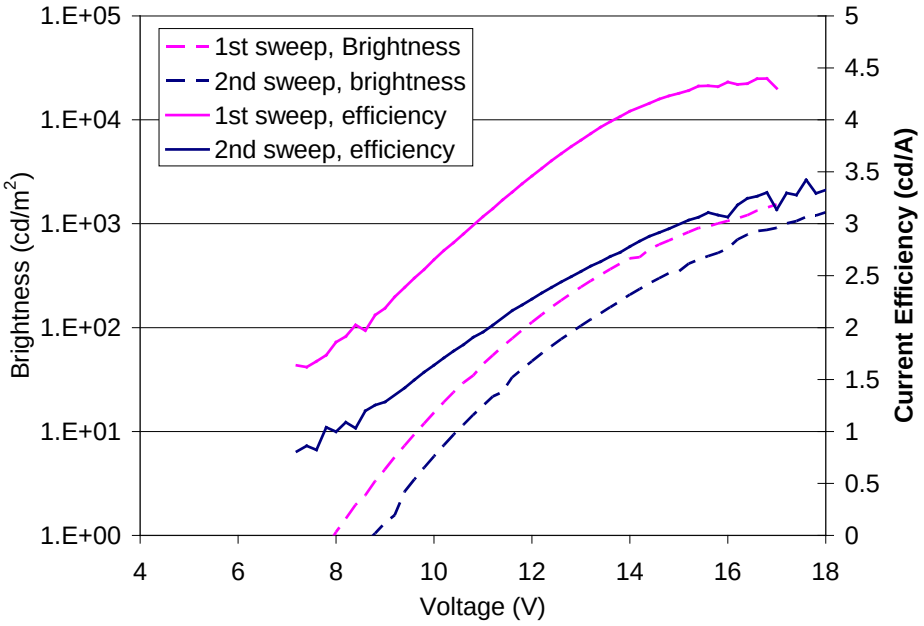


Figure 2-10. Performance of HLED devices combining a transparent oxide cathode and a doped organic buffer layer.

v. Inverted HLED stability

Preliminary tests were conducted to evaluate the original hypothesis that HLEDs, by eliminating the low work function metal cathode, would be more robust to environmental degradation than standard OLEDs. Generally speaking there are two modes of OLED degradation. One is simple molecular instability of the substituent materials under electro-photo-excitation. In this regard, OLEDs have become very robust devices, often operating for >100,000 under ideal conditions. The second mode of failure is through chemical attack due primarily to reaction with water. This is the primary hurdle for flexible OLED-based displays on polymer substrates. This mode of degradation is easily identified by characteristic "dark spot" formation and growth and/or pixel shrinkage. While the former degradation mode leads to gradual, uniformly lower emission intensities, dark spot formation is observed visually as local regions where no emission

occurs. This degradation occurs by a fairly complex mechanism, but can be summarized as a local region where delamination between the metal cathode and the anode occurs. Where delamination occurs, no current flows and this is observed as a dark spot. This occurs near defects, and as moisture penetration continues, the dark spots increase in size/area.

The stability of HLEDs was evaluated by fabricating HLEDs and standard OLEDs, removing them from the inert ambient of the glove box without any encapsulation, and periodically monitoring the dark spot formation and growth. Figure 2-11 shows the results and demonstrates that there is no substantial difference in environmental stability of the HLEDs vs. the OLEDs.

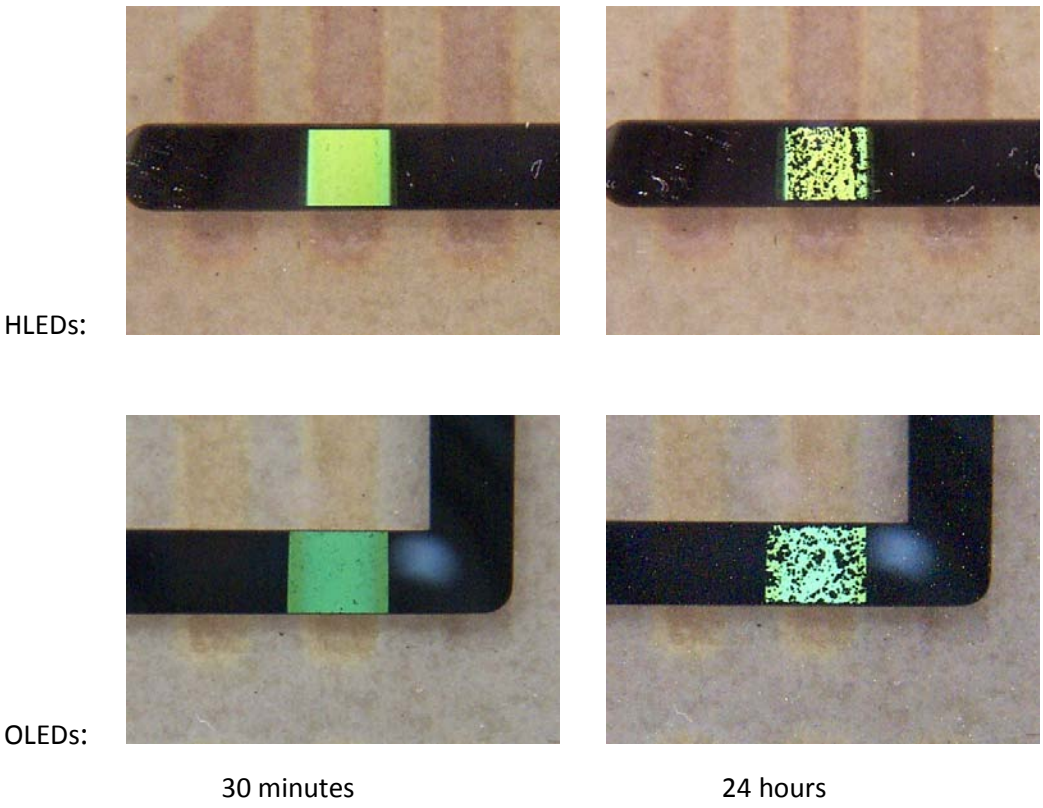


Figure 2-11. Dark spot growth over time for HLEDs and OLEDs.

To more clearly identify whether the dark spots occurred due to delamination of the metal anode vs. the oxide cathode, we looked at the samples using differential interference contrast (DIC) microscopy to highlight texture in the samples. Figure 2-12 shows a representative DIC image of an HLED sample after 24 hours exposure to ambient conditions. Bubbling that correlates to dark spots is clearly observed. Moreover, this delamination could be observed in regions where there was no underlying cathode, clearly indicating that the delamination occurs between the Al anode and the underlying organic layers.

Figure 2-12. DIC image of an HLED sample after 24hrs exposure to ambient conditions.

To summarize, these results show that there is substantial promise for improving the environmental stability and performance of HLEDs. Standard OLED structures are very limited in the selection of cathode materials, requiring reactive, low melting temperature metals. We have shown that Al anodes delaminate just like Al cathodes, which is not overly surprising. The benefit to the inverted HLED structure is that there is substantially more freedom in the selection of anode materials than cathode materials. These materials would be the basis of research in subsequent years.

vi. Molecular Functionalization of Inorganic Semiconductors

In Year 3 a glove box was purchased and installed at NCA&TSU (Figure 2-13) and the depositions in the inert ambient were entirely carried out at NCA&TSU.

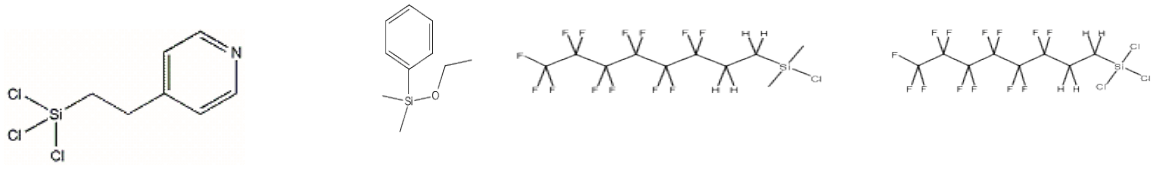
Figure 2-13. Photograph of glove box at NCA&TSU.

In year 2 we had demonstrated SAMs coverage was successful only from PFPTO, but not from BTO or DPDMO using the solution processing. This year a series of organic molecules was examined for SAM functionalization of reference Si substrates. The promising monolayers were then deposited on ZnO:Al electrodes.deposited in ARL labs. Success of this phase is to identify the precursors that have the ability to deposit a monolayer. The monolayer deposition is characterized using contact angle measurements and coverage of the monolayer is implied when the contact angle exhibits saturation with longer deposition times.

SAM formation on Si and ZnO:Al substrates was performed by the dipping technique outlined in the last section. Table 2-8 lists the pertinent information on the precursors that were examined during this year, and the molecular structures are shown in Figure 2-30. Substrates were placed in the precursor solution in jars that were sealed and placed in an oven for times ranging from 30 to 120 minutes and temperatures from 25 to 70°C, and were rinsed in methanol after processing. Control samples underwent the same procedure, but with no precursor dissolved in the toluene.

Table 2-8. Precursor #, names and boiling points for the surface modifiers used in this study.

Precursor #	Name	Boiling point (°C)	Drawing
1	4-[2-(Trichlorosilyl)ethyl]pyridine 15-20%	110	a
2	Phenyldimethylethoxysilane	93 at 25mm	b
3	(Tridecafluoro-1,1,2,2-tetrahydrooctyl)dimethychlorosilane	189-191	c
4	(Tridecafluoro-1,1,2,2-tetrahydrooctyl)trichlorosilane	84-85 at 17mm	d



(a) (b) (c) (d)

Figure 2-30. Molecular structure for the surface modifiers used in this study.

Precursor 1: 4-[2-(Trichlorosilyl)ethyl]pyridine 15-20%

Figure 2-31 shows the contact angle of 4-[2-(Trichlorosilyl)ethyl]pyridine 15-20% SAMs as a function of time for different temperatures. Control samples varied from 21°C to 41°C and therefore are denoted by the dashed lines. The results showed that regardless of temperature and time, little systematic modification of the contact angle was observed.

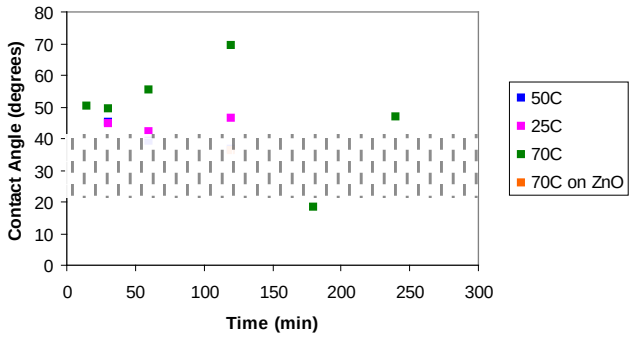


Figure 2-31. 4-[2-(Trichlorosilyl)ethyl]pyridine 15-20% (precursor 1) contact angle as a function of immersion time at temperatures of ( ) 25°C on Si, ( ) 50°C on Si, ( ) 70°C on Si, and ( ) 70°C on ZnO.

Precursor 2: Phenyldimethylethoxysilane

Figure 2-32 shows contact angle results for Phenyldimethylethoxysilane (precursor 2) at various temperatures as a function of time. Only the samples deposited at 70°C indicated an increase in the contact angle though did not exhibit any saturation in the deposition duration investigated.

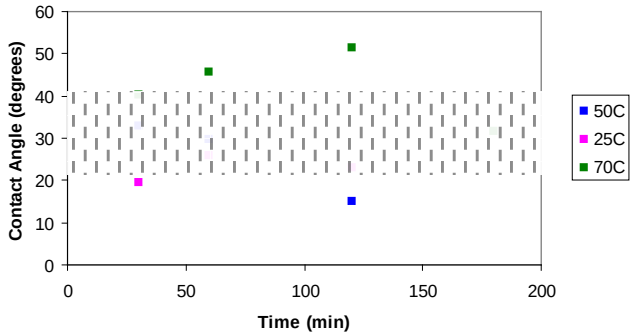


Figure 2-32. Phenyldimethylethoxysilane (precursor 2), contact angle as a function of immersion time at temperatures of ( ) 25°C on Si, ( ) 50°C on Si, ( ) 70°C on Si.

Precursor 3: (Tridecafluoro-1,1,2,2-tetrahydrooctyl) dimethychlorosilane

(Tridecafluoro-1,1,2,2-tetrahydrooctyl)dimethychlorosilane (precursor 3) at 1mM for various times and temperatures is demonstrated in Figure 2-14. Samples dipped in this precursor displayed higher contact angle and saturation only for 70°C processing indicative of the conditions being favorable for monolayer formation.

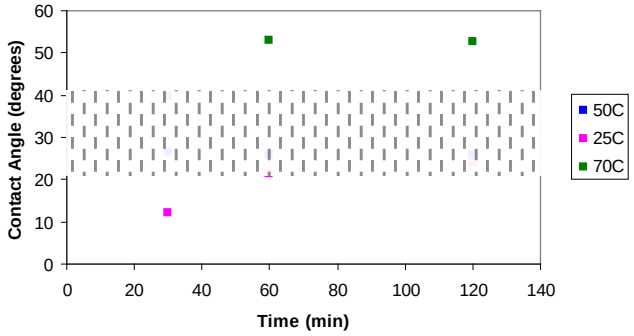


Figure 2-14. (Tridecafluoro-1,1,2,2-tetrahydrooctyl)dimethychlorosilane (precursor 3) contact angle as a function of immersion time at temperatures of ( ) 25°C on Si, ( ) 50°C on Si, ( ) 70°C on Si.

Precursor 4: (Tridecafluoro-1,1,2,2-tetrahydrooctyl) Trichlorosilane

(Tridecafluoro-1,1,2,2-tetrahydrooctyl)trichlorosilane (precursor 4) at 1mM for various times and temperatures is demonstrated in Figure 2-15. Samples dipped in precursor 4 showed

higher contact angles and exhibited saturation above 40 minutes for all the temperatures investigated. All angles were above the control range indicating that even at room temperature a monolayer was capable of being deposited.

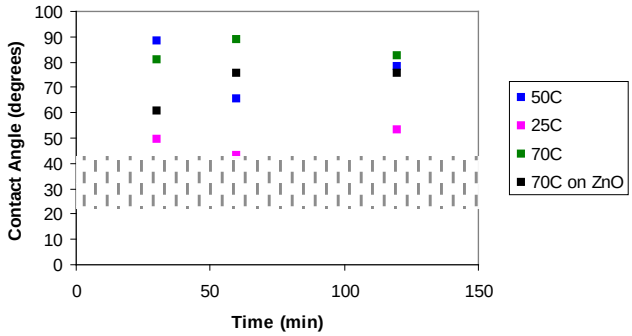


Figure 2-15. (Tridecafluoro-1,1,2,2-tetrahydrooctyl)trichlorosilane (precursor 4) contact angle as a function of immersion time at temperatures of (■) 25°C on Si, (■) 50°C on Si, (■) 70°C on Si, and (■) 70°C on ZnO:Al.

70° C Contact Angle Results

Amongst the different precursors studied precursors 3 & 4 showed the most promise in terms of layer formation and a deposition temperature of 70°C appears to be the optimum temperature of deposition. The contact angle for precursors 1 thru 4 deposited at 70°C is demonstrated in Figure 2-16. Precursor 4 deposited on both Si and ZnO:Al show a similar trend, but the ZnO:Al deposition has noticeably lower contact angles, also precursor 1 deposited on ZnO:Al for 120 minutes is significantly lower than on the Si deposited for the same time. Though monolayer coverage is found to be successful on ZnO:Al , the surface energy appears to be lower than the Si surface.

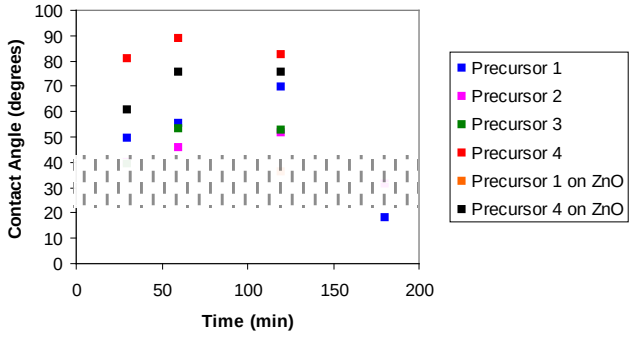


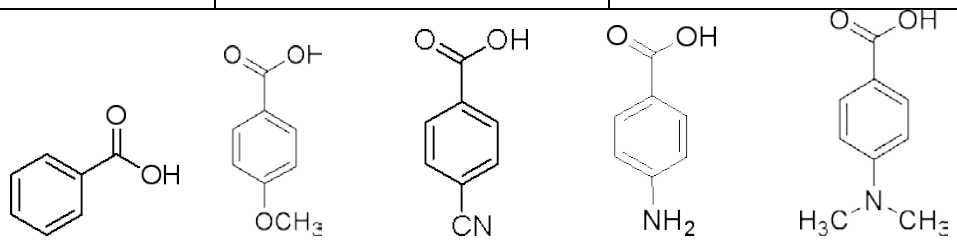
Figure 2-16. Contact angle as a function of immersion time at temperatures of (■) Precursor 1 on Si, (■) Precursor 2 on Si, (■) Precursor 3on Si, (■) Precursor 4 on Si, (■) Precursor 1 on ZnO:Al and (■) Precursor 4 on ZnO:Al.

Benzoic Acid Derivatives.

We then began the investigation of five new precursors, all of which are benzoic acid derivatives. Name and melting point, and molecular structure are given in Figure 2-17 and Table **2-9**, respectively.

Table 2-9. Precursor #, names and boiling points for the surface modifiers used in this study.

Name	Melting Point °C	Drawing
Benzoic Acid	121-125	a
P-Anisic Acid	182	b
4-Cyanobenzoic Acid	219	c
4-Aminobenzoic Acid	186	d
4-(Dimethylamino) Benzoic Acid	243	e



(a) (b) (c) (d) (e)

Figure 2-17. Molecular structure for the benzoic acid derivatives used in this study, namely, (a) benzoic acid, (b) p-anisic acid, (c) 4-cyanobenzoic acid, (d) 4-aminobenzoic acid, and (e) 4-(dimethylamino)benzoic acid.

The precursors were dissolved in acetonitrile at concentrations of 5 mM and stored in the glove box under the N ambient to prevent degradation of the precursors. Substrates were placed in the precursor solution in jars that were sealed and left in the glove box for times ranging from 30 to 120 minutes, and were then rinsed in acetonitrile after processing. The films were characterized using contact angle.

Samples dipped in Benzoic Acid follow the same trend as the previous precursors. The saturation at shown by the contact angles of 60 and 120 minute depositions in Figure 2-18 illustrates that a monolayer has been deposited. Samples dipped in 4-aminobenzoic acid illustrate a different trend with a marginal decrease in contact angle with time indicating organic residue was left over for longer deposition duration. These preliminary experiments must be extended to understand the surface energies and resulting contact angles expected for benzoic acid monolayers. XPS may be used to confirm the presence or absence of these monolayers.

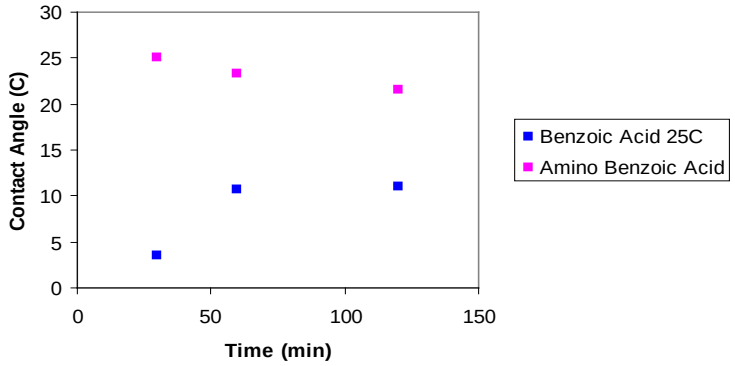


Figure 2-18. Contact angle as a function of immersion time (■) Benzoic Acid 25°C, (■) Amino Benzoic Acid 25°C.

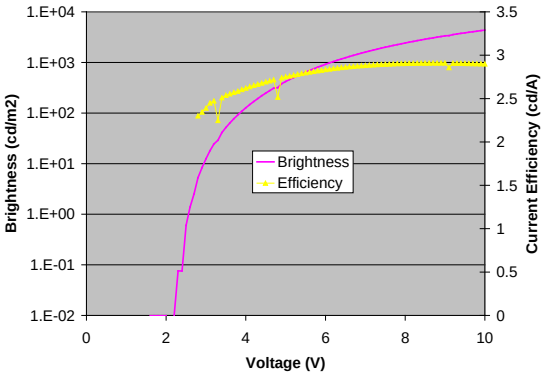
Year 4

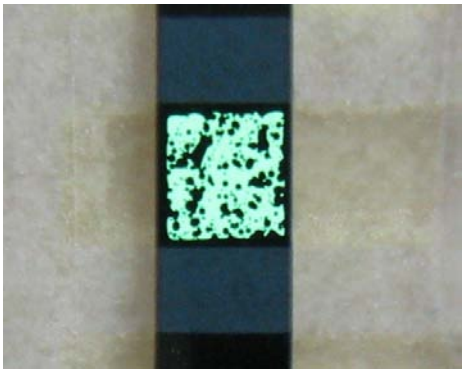
i. Devices with Reduced Dark Spot Growth

The plan during Year 4 to reduce dark spot growth was based on improving adhesion between the anode and the organic layers. As demonstrated in Year 3, aluminum metal on organic layers, even in an inverted structure and with no reactive metal component, shows blistering and delamination from the organics. However, the most interesting observation from the effort to develop an inverted device structure was the ability to fabricate an efficient device using an oxide buffer layer. It is well known that easily oxidized metals such as aluminum have good adhesion to oxide substrates. So the initial plan was to demonstrate improved resistance to dark spot formation using an Al/MoO_3 interface. Initial experiments showed that device performance was minimally affected when the MoO_3 layer thickness increased from 50Å to 250Å, so this allows a complete oxide layer to be formed.

ii. Evaluation of Dark Spot Growth

A standard OLED device was fabricated and digital images taken over time. Unless otherwise noted, all dark spot growth experiments were performed by leaving the device in air without encapsulation, and without operation. The device was activated for periodic digital images to observe dark spots. Two primary factors are observed during these tests. First, the qualitative growth of dark spots is observed. Second, the shrinkage of the active region near the edge of the electrodes ("pixel shrinkage") is observed for both vertical and horizontal edges. Both types of evaluation can be quantified but have not been for this study. Figure 2-19 shows the brightness, efficiency, and dark spot growth for the standard device, which consists of ITO / CF_4 plasma treated surface / 400Å N PB / 600Å Alq_3 / 8Å LiF / 500Å Al / 500Å Ag. (Note: the Al/Ag metal stack is not necessary, but simplifies our ability to consistently achieve 1000Å of metal.) These data are useful in evaluating the relative performance of the new device structures.



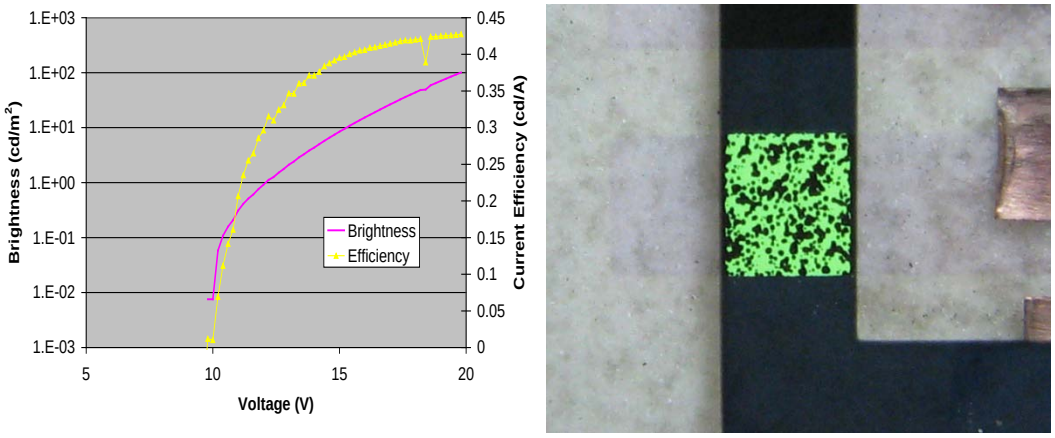


(A) (B)

Figure 2-19. (A) Device performance and (B) dark spot growth for a standard OLED device after 48 hours.

iii. Standard (Non-Inverted) Devices with Adhesion Layer

Preliminary experiments were performed using a non-inverted structure. Several devices were fabricated with the following structure as the baseline: ITO / 150Å CuPc / 400Å NPB / 600Å Alq_3 / 150Å BCP / 200Å MoO_3 / 500Å Al / 500Å Ag. The best non-inverted performance was achieved by replacing the CuPc hole-injection layer with a CF_4 plasma treatment, which resulted in high operating voltage, but also high efficiency, as shown in Figure 2-20. The dark spot growth was comparable to the standard device, but there was noticeable reduction in pixel shrinkage.

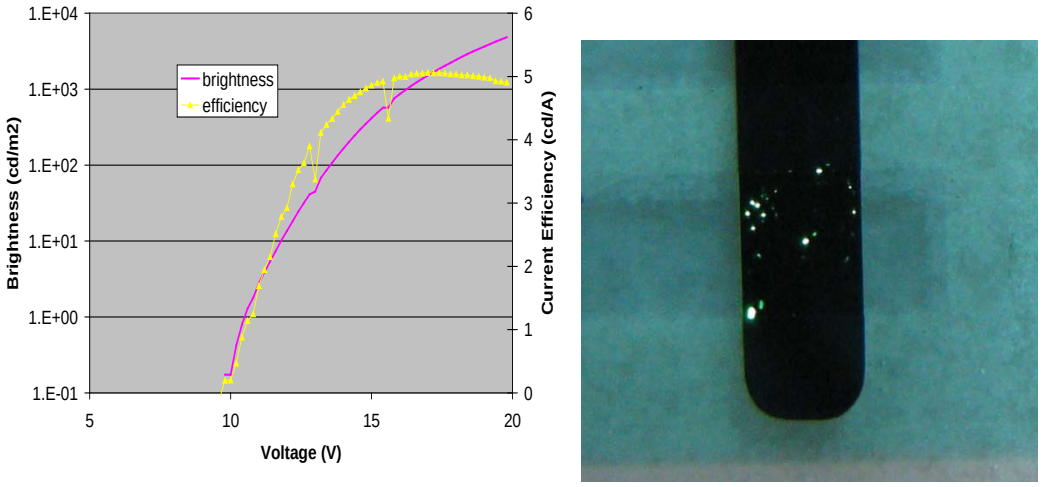


(A) (B)

Figure 2-20. (A) Device performance for a non-inverted OLED with MoO_3 adhesion layer and (B) dark spot growth after 72 hours.

iv. Inverted Devices with Adhesion Layer

Inverted devices with a similar structure to those developed in Year 3 were evaluated with regard to dark spot growth using MoO_3 adhesion layers. Initial devices utilized a CuPc buffer layer between the NPB hole transport layer and the MoO_3 adhesion layer. Figure 2-40 shows high operating voltage and high efficiency. However after 24 hours the device area was almost completely inoperable.

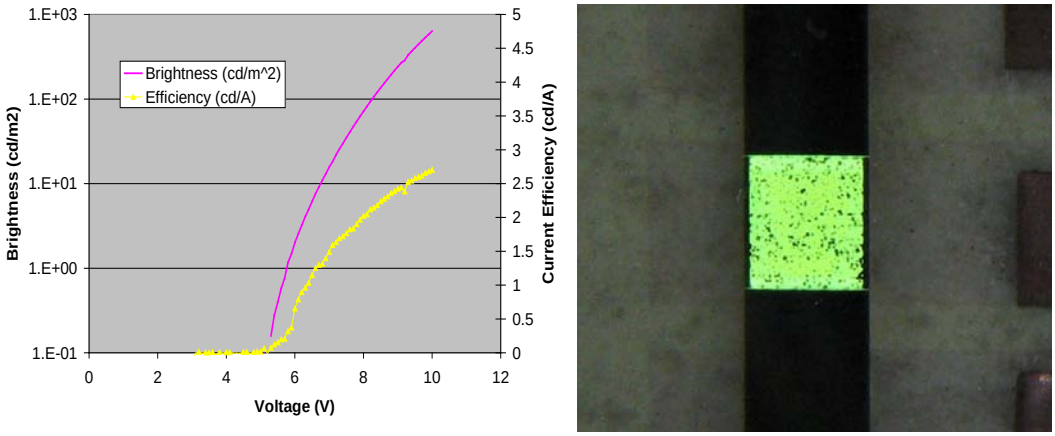


(A) (B)

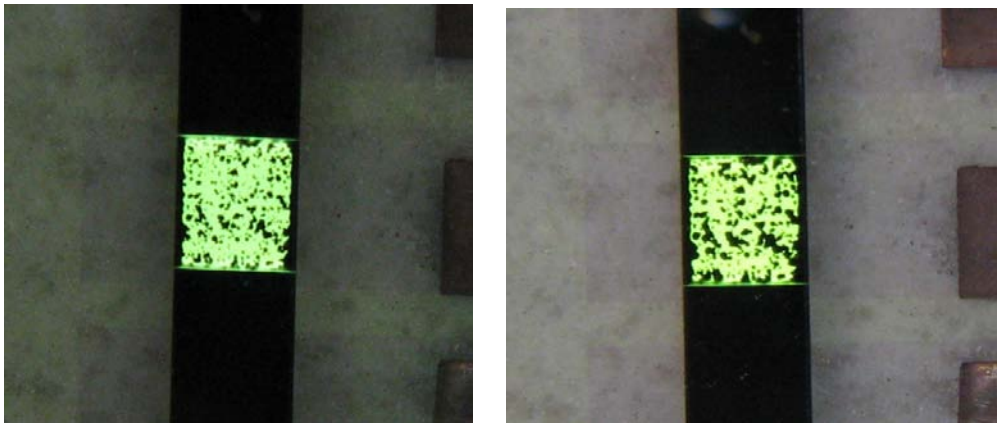
Figure 2-40. (A) Device performance for an inverted OLED with CuPc and MoO_3 adhesion layer and (B) dark spot growth after 24 hours.

v. High Performance, Stable Inverted Devices

A major step forward was achieved when two additional changes were made to the device structure. First, a thin layer of Ca was deposited onto the oxide cathode. Similar performance was observed with a thin layer of ZnO:H (for details, see report for Year 3), vs. Ca directly on ITO. For an unencapsulated device, the Ca layer will quickly form a mixture of CaO and $Ca(OH)_2$. However, CaO is known to be a low work function material, while the properties of $Ca(OH)_2$ are not known. Second, the hole injection layer was eliminated and the MoO_3 adhesion layer was deposited directly onto a thicker (700Å) NPB hole transport layer. Several variations on this approach were evaluated. The final structure was based on ITO / 100Å Ca / 150Å BCP / 450Å Alq_3 / 700Å NPB / 150Å MoO_3 / 500Å Al / 500Å Ag. Figure 2-41 shows the performance of this a device using this structure as well as the dark spot growth. Clearly a substantial reduction in dark spot growth has been achieved. Figure 2-42 highlights a comparison of the reference OLED after 48 hours with the above device structure after 2 weeks. Interestingly, we frequently observed that the horizontal edges of these devices hardly degrade. We will discuss this feature in the following section. Further, we evaluated several variations on the cathode injection stack. In general, these variations did affect device efficiency but generally had little effect on operating voltage and dark spot growth. A significant limitation of this device structure has been observed. While encapsulated devices operate stably under constant operation, unencapsulated devices do not. These devices tend to result in electrical shorting after ~2-4 hours of constant operation at a moderate brightness levels (~500 cd/m^2). This will also be discussed in the following section.



(A) (B)



i. (D)

Figure 2-41. (A) Device performance for an inverted OLED with Ca/ITO cathode and NPB/MoO_3 adhesion layer and dark spot growth after (B) 1 week, (C) 2 weeks, and (D) 3 weeks.

(A) (B)

Figure 2-42. (A) Dark spot growth comparison for (A) a reference OLED after 48 hours and (B) an improved inverted OLED after 2 weeks.

vi. Discussion

The use of NPB / MoO_3 / Al as an anode interface with improved adhesion has been shown to reduce the growth of dark spots in inverted OLED devices. However at this point there were many questions to be answered. The organic/oxide/metal structure does not seem to be a generic solution. The adhesion seems to be highly dependent on the selection of the hole-injection organic. There is little understanding of what makes a good organic/oxide couple and at this point the selection is empirical.

Improved adhesion does not appear to have a substantial effect on the density of dark spots. Previous published reports have indicated that while dark spots are caused by delamination of the top metal from the organic, they actually originate due to surface features at the bottom oxide. It may be possible to combine bottom electrode surface treatments with the improved adhesion.

There are two interesting but poorly understood features that may be exploited to further improve degradation. One is the difference in pixel shrinkage on the oxide edge vs. the metal edge. On both edges pixel shrinkage is dramatically reduced compared with a standard OLED. But the differential between edges is not a consistent feature and should be explored and exploited to eliminate pixel shrinkage. Second, there is typically a line feature at the Ca edge where degradation is substantially lower than the rest of the device. This is seen in Figure 2-21. The mask geometry is such that the Ca does not extend completely to the edge of the ITO, but emission is only observed to the edge of the Ca, so this feature is at the edge of a 100 Å layer of Ca. This is also poorly understood but could potentially be exploited for improved degradation performance.

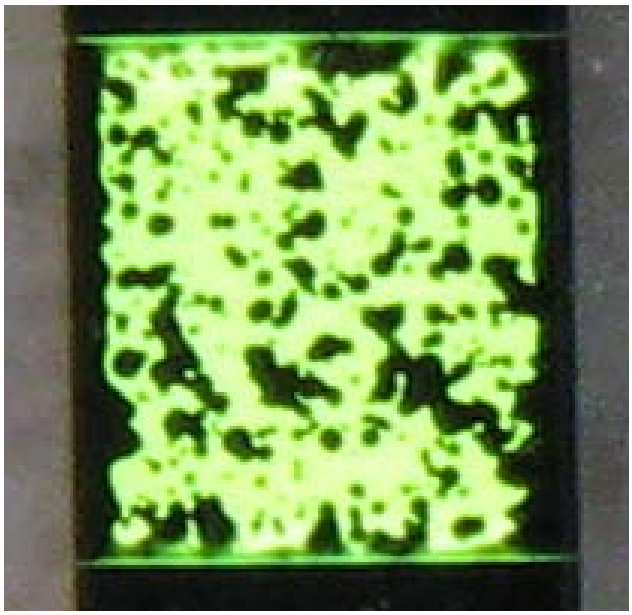


Figure 2-21. Close-up of device after 3 weeks of ambient storage. Reduced degradation at the horizontal edges is clear.

A critical shortcoming of the devices in their current version are that constant operation results in electrical shorting after a few hours of operation. Figure 2-22 shows the voltage as a function of time for a device operating under constant 1 mA/cm^2 current. Future experiments would be conducted to investigate the source of this failure. Possibilities include migration of the MoO_3 or the $Ca(OH)_2$, leading to filamentary conduction and shorting.

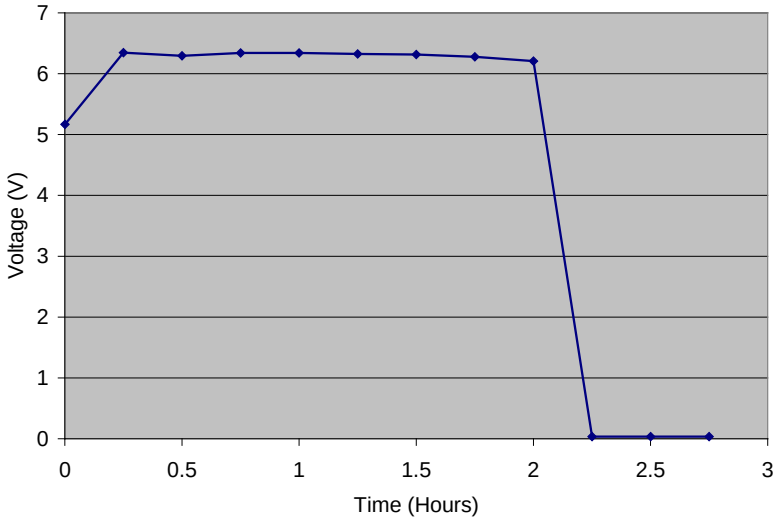


Figure 2-22. Operating voltage vs. time for a degradation-resistant device under constant operation.

Finally, it should be noted that the experiments to date were intended to evaluate large effects on degradation and operating voltage, but very little optimization has been performed. Once a stable, degradation-resistant structure is identified, it is anticipated that (a) performance increases due to device optimization may be achieved, and (b) additional device engineering, including highly efficient doped emitters may be integrated to provide improved efficiency without affecting dark spot formation.

Year 5

Utilizing the inverted, hybrid structure developed in previous years, we attempted to understand and mitigate the formation of dark spots, as well as to improve device performance and stability. We were able to achieve device lifetimes that exceeded 500 hours of continuous operation with no encapsulation, and lifetimes exceeding 1000 hours without operation.

The device lifetimes reported in Year 4 were poor, with devices experiencing shorting within a few hours of operation. In an effort to understand the culprit(s) responsible for early device failure (anode buffer migration, cathode buffer migration, etc), an experiment was designed to start with a basic hole- or electron-only structure. Each successive layer was then added, finally reaching a complete device structure using the inverted hybrid device as shown in Figure 2-23 (ITO / 100 Å cathode buffer / 150 Å BCP / 450 Å Alq_3 / 700 Å NPB / 150 Å anode buffer / 1000 Å Al). For the purpose of the report, the anode buffer will be referred to as AB, and the cathode buffer as CB

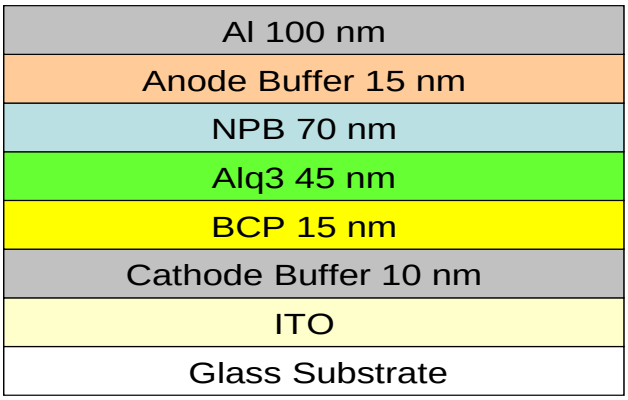


Figure 2-23. Device structure for IOLEDs used in the stability study.

The samples were designated and fabricated as follows, and Figure 2-24 shows the current-voltage characteristics for these devices:

1196B: ITO / 150 Å BCP/ 450 Å Alq3/ 700 Å NPB/ 150 Å AB/ 500 Å Al / 500 Å Ag
1204A: ITO / 100Å CB/ 150Å BCP/ 450Å Alq3/ 1000Å Al
1204B: ITO / 100Å CB/ 150Å BCP/ 450Å Alq3/ 700Å NPB/ 1000Å Al
1204C: ITO / 100Å CB/ 150Å BCP/ 450Å Alq3/ 700Å NPB/ 150Å AB/ 1000Å Al
1204D: ITO / 100Å CB/ 150Å BCP/ 450Å Alq3/ 700Å NPB/ 150Å AB/ 1000Å Al
1206A: ITO / 150Å BCP/ 450Å Alq3/ 700Å NPB/ 150Å AB/ 1000Å Al
1206B: ITO / 450Å Alq3/ 700Å NPB/ 150 Å AB/ 1000Å Al
1206C: ITO / 700Å NPB/ 150Å AB/ 1000Å Al

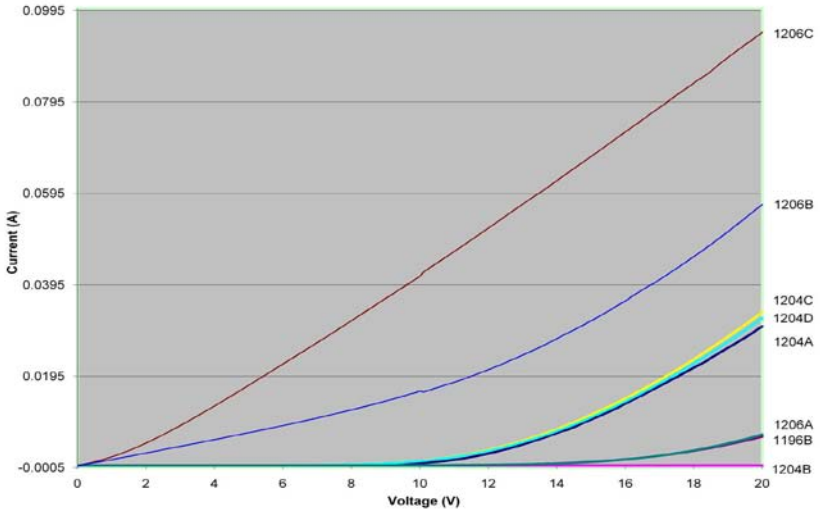


Figure 2-24. Current – Voltage data for stability study devices.

By design, some of these structures are efficient for only one carrier type. Due to the resulting carrier imbalance, not every device emitted light. But evaluating stability under constant current conditions can give an indication of which materials may be the source of shorting. Sample 1206C is designed to inject/transport only holes ("hole-only"), and the I-V data serves as evidence that the AB – Al interface is an efficient anode. The lack of current in 1204B, even at high voltages, demonstrates the necessity of the AB layer for an efficient anode. Samples 1196B and 1206A demonstrate the inefficient charge injection from ITO into BCP, which is expected. Comparing 1204A with 1204C and 1204D demonstrates that the device current is limited by cathode injection. Sample 1204A is an electron-only device, and the addition of an efficient anode in 1204C and 1204D provides no additional current. In conclusion, the electrical performance of the inverted anode appears to be quite good with moderate operating voltage. The addition of the CB improves cathode performance, but is still the limiting factor in low voltage operation, and an improved cathode structure is necessary.

Two different device stability tests were performed. Some devices were operated under constant current conditions, while voltage output was monitored and images were periodically collected to monitor dark spot growth. Other devices were operated only intermittently to collect images of dark spot growth, but were otherwise stored in ambient conditions. In both cases, no encapsulation of the devices was used; they were completely exposed to ambient oxygen and moisture.

Figure 2-25 shows the voltage over time for 3 devices operated under constant current. Sample 1204C (blue curve) was a full inverted device with a CB layer at the cathode and AB at the anode. Sample 1206A (black curve) is the same device structure without a CB, and it was therefore necessary to lower the current density for the device to operate at a reasonable voltage. Sample 1204B (red curve) is the same device structure without the AB layer. It was found that the most rapid degradation occurred in the sample with no CB layer. However, this sample also experienced the most heating during the test, due to the lower efficiency of the device. The sample with no AB was very stable, but the very low current density did not provide the same electrical stress experienced by the other devices. The full device was moderately stable for ~230 hours before the degradation rate increased rapidly. Unlike previous tests, the degradation was gradual; no shorting occurred. These results clearly indicate the importance of the presence of injection layers at both the anode and cathode, but were not conclusive with respect to the primary cause for degradation. The lack of shorting defects suggest that previous failures may have been due to surface roughness, particulates, or some other physical structure that led to field concentration. Future tests are planned in which similar electrical stress is applied to the sample during testing.

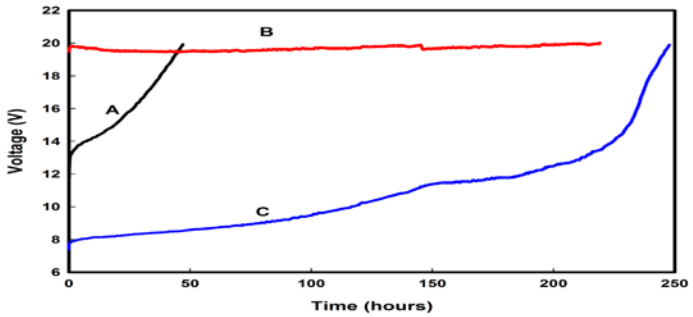
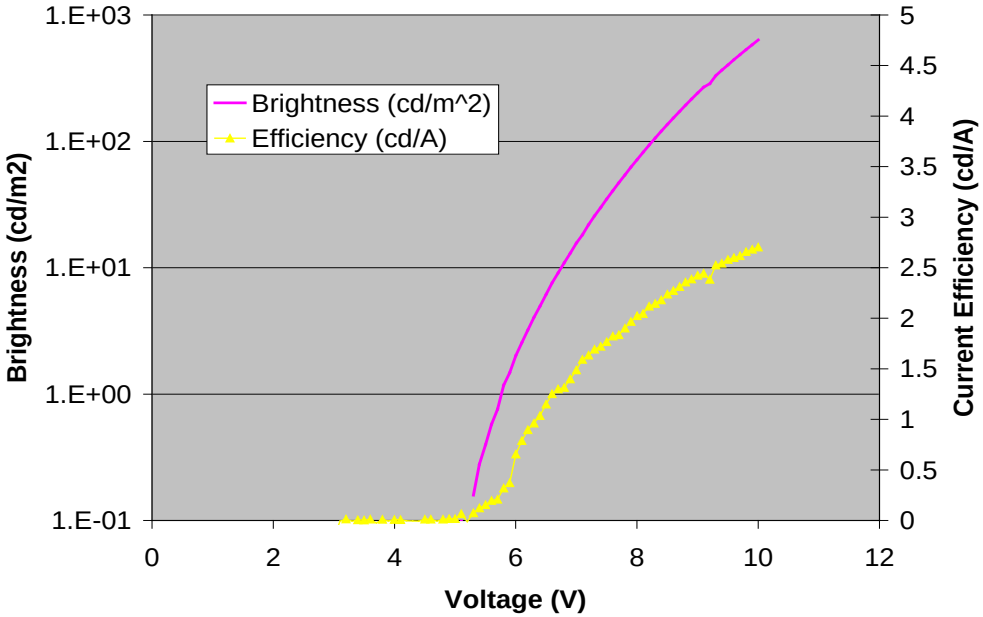
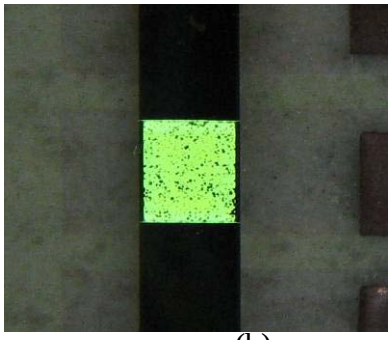


Figure 2-25. Voltage at a constant bias as a function of time for A) 1206A (Full device, no CB, 0.1 mA), B) 1204B (full device, no AB, 0.01 mA), C) 1204C (full device, 0.1 mA).

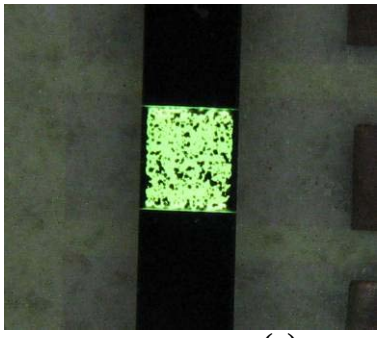
The second type of degradation study involved ambient aging of unencapsulated devices, with periodic evaluation. In this case, the best overall device performance considering efficiency, operating voltage, and dark spot growth, came from the full inverted structure with CB and AB injection layers. Figure 2-26(a) shows the I-V and efficiency-voltage characteristics for the full device. The images in Figure 2-26(b-d) show the device after 1, 2 and 3 weeks (~500 hours) of aging, respectively. The dark spot density is typical for OLED device structures. The unique aspect of these devices is the extremely slow growth of the dark spots, attributed to the improved adhesion between the AB injection layer and the Al anode.



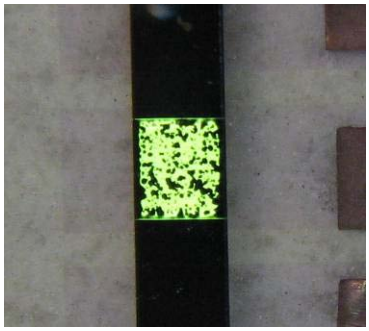
(a)



(b)



(c)

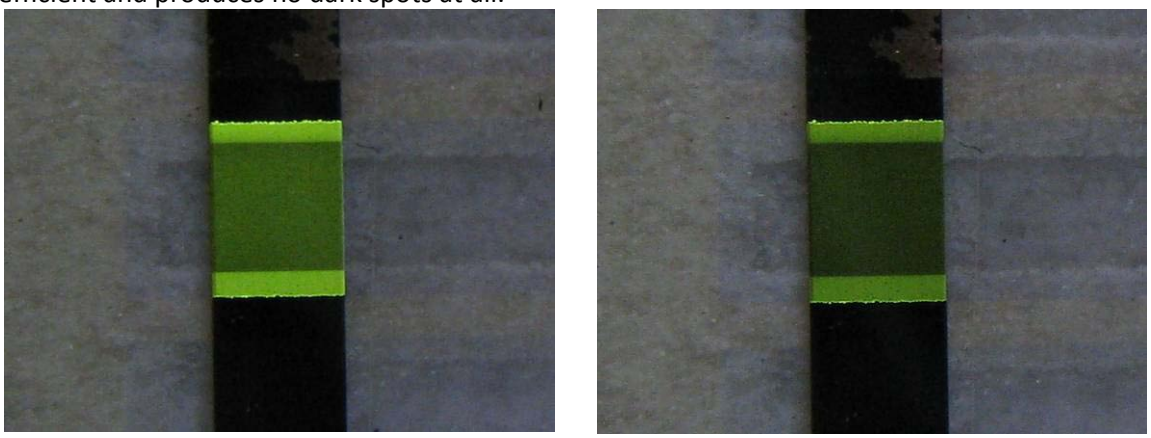


(d)

Figure 2-26. (a) Current and efficiency vs. voltage for the full inverted structure. Images of dark spot growth for the same device taken after (b) 1 week, (c) 2 weeks and (d) 3 weeks of ambient aging.

Another interesting result was from a similar device with a thinner CB injection layer, or no injection layer at all. As mentioned previously, the CB layer (or some replacement for it) is necessary for efficient electron injection. But we have seen in repeated studies that devices with no CB layer, while operating at high voltage, exhibit little or no dark spot formation. Figure 2-27(a) and (b) show images of a device with a thinner 20 Å CB layer at 5 and 6 weeks (~1000

hours) of ambient storage, respectively. It is interesting to note that the region with the CB becomes less efficient over time than the brighter regions that had no CB at all. Both regions show the lack of dark spot formation, making the thicker CB used in the standard structure most probable source of dark spots. It also opens the possibility of finding a suitable injection layer that is both efficient and produces no dark spots at all.



(a) (b)

Figure 2-27. Pictures of a device with a thin, 20Å CB, after (a) 5 weeks and (b) 6 weeks of ambient storage.

i. Cathode Modification / Novel Cathodes

The plan to reduce dark spot formation was based on modifying the interface of the oxide cathode with the organic electron injection / hole blocking layer. Compared to a similar device that does not have the CB layer, the addition of the CB results in significantly reduced operating voltage and increased efficiency, but also a higher density of dark spots. The goal of subsequent work was to identify a replacement CB layer. The first material chosen was cesium carbonate, Cs_2CO_3. Cesium carbonate has been shown to decrease the work function of ITO from 4.6 eV to <3 eV using a very thin interfacial layer, although published efforts only measured work function and did not demonstrate low voltage devices. Devices with differing thicknesses of the cesium carbonate layer were fabricated. The brightness of the devices for a given forward current was improved, compared to devices with the traditional CB, but at the cost of higher operating voltages. Figure 2-50 shows the initial devices images and dark spot growth after 1 week of continuous operation respectively for devices using (a, b) the traditional CB injection layer, (c, d) a 10 Å Cs_2CO_3 injection layer and (e, f) a 20 Å Cs_2CO_3 injection layer. Device stability for the thinnest (10 Å) layer was slightly improved over the no-CB containing device, showing a reduced rate of dark spot growth. However, dark spot growth for the thickest (20 Å) layer was significantly higher. Further experiments were planned to determine the effect of annealing of the cesium carbonate layer on device performance and lifetime.

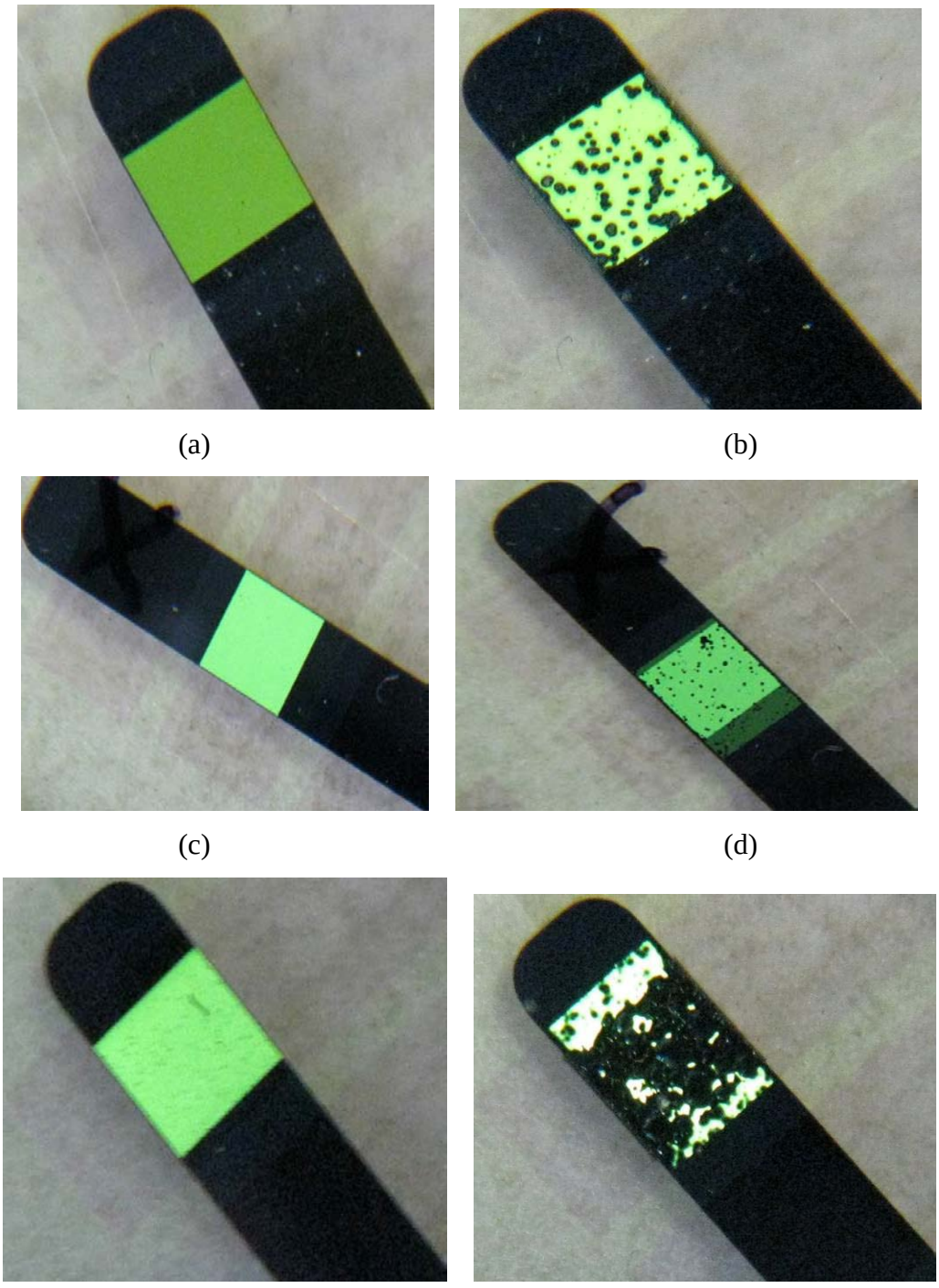


Figure 2-50. (a) 1218A CB device at time = 0, (b) CB device at time = 1 week, (c) Cs_2CO_3 device (10 Å) at time = 0, (d) Cs_2CO_3 device (10 Å) at time = 1 week, (e) Cs_2CO_3 device (20 Å) at time = 0, (f) Cs_2CO_3 device (20 Å) at time = 1 week.

The use of organophosponic acids has also been used to demonstrate a reduced work function for ITO. Several papers have shown a reduction of more than 2 eV. This reduced injection barrier would be expected to lead to more efficient devices with lower operating voltage. Several experiments were conducted using an octylphosponic acid (OPA) surface monolayer functionalization fabricated according to published procedures. Electron only devices (ITO/OPA/BCP/Alq_3/Al) were fabricated, and an increase in electron injection / transport was observed, but device breakdown occurred at a low voltage of ~8 V. It was hypothesized that the surface was not sufficiently clean after monolayer deposition, which resulted in device shorting. Experiments were planned to evaluate this hypothesis and remedy the problem.

ii. Discussion

Studies to understand the failure mechanism and formation of black spots were partially conclusive. These studies did not unequivocally show whether migration of oxide species is the majority factor in device failure. Devices which do not contain the CB layer and devices which do not contain the AB layer operate as long as devices which contain these materials, and failure was gradual. This indicates that previous shorting failures were caused by physical imperfections (roughness, particles, surface contaminants, etc.). Further optimization of device design and materials thicknesses is necessary to understand the reason for failure and will be undertaken in the future.

Studies with reduced CB layer thickness show an intriguing result, where dark spots do not form over periods of weeks. This offers the hope of finding an appropriate injection layer that provides efficient charge injection, but does not induce dark spot formation.

It also appears that device operating efficiency is greatly affected by the large energy difference at the ITO/organic interface. Cesium carbonate should have helped by lowering this barrier, but morphological effects appeared and caused device failure.

Year 6

i. Operating Voltage

A layer schematic of the inverted, hybrid OLED structure developed in previous years is shown in Figure 2-51. The high operating voltage of the hybrid OLED device (> 7 Volts) is primarily limited by the poor electron injection properties of ITO. ITO has a work function of ~4.6eV, which does not provide efficient electron injection into the device stack. To overcome this barrier, an increased driving force is required, resulting in a higher operating voltage. Calcium helps lower this barrier, but does not reach the target value for mainstream OLEDs of < 5 V. This year's focus has been on modifying the cathode to lower the operating voltage, while maintaining decent device lifetime. Four approaches were evaluated, but the use of lithium quinolate (LiQ) as a hole blocker and electron injection layer, and the use of with the use of p-anisic acid (4-methoxybenzoic acid)-treated ZnO cathodes were inconclusive, and require further research. The results for annealed Cs_2O_3 and oxidized Ca CB layers are outlined below.

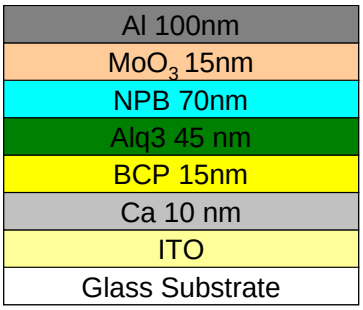


Figure 2-51. Device structure for inverted organic light emitting diode (IOLED).

Ca does reduce the operating voltage and increases efficiency, when compared to devices without Ca, but results in higher defect density and earlier device failure. This is primarily due to the fact that Ca, when exposed to moisture and oxygen, is chemically converted to CaO and $Ca(OH)_2$ species. The last report mentioned work with cesium carbonate (Cs_2CO_3). Cs_2CO_3 does reduce the work function of ITO from 4.6eV to ~ 3eV, but is not a conductive layer unless it decomposes, leaving Cs as a dopant. Devices fabricated with varying Cs_2CO_3 thicknesses did improve brightness, but the devices showed visible regions of inoperability, shown in Figure 2-50, and did not improve operating voltage. This is sometimes seen when a thin insulating layer is placed at the ITO-organic interface. Another possibility is that the morphology of the Cs_2CO_3 at the ITO interface was the culprit in the poor device performance.

We evaluated whether annealing could provide decomposition of the $CsCO_3$ layer, or could modify the morphology to improve device properties. Samples were prepared with varying thicknesses of Cs_2CO and these samples were then annealed at 150°C for 20 min under inert atmosphere. The images in Figure 2-52 show that annealing did reduce the striated dark regions, but did not significantly improve device efficiency or operating voltage. The resulting devices showed a turn-on voltage of ~9V (Ca ~7V, ITO Only ~10V) with a maximum efficiency of 1.2cd / A and a maximum brightness of 260 cd/m^2. Lifetimes of the annealed devices were significantly shorter that Ca- or ITO-only devices, with devices shorting in less than 1 hour.

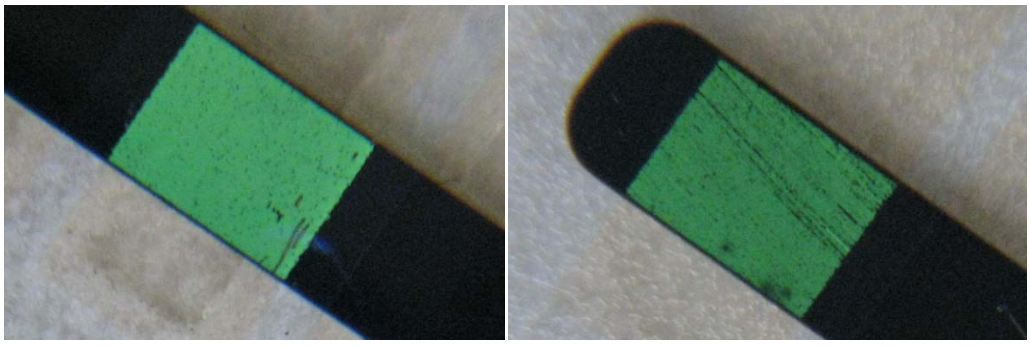


Figure 2-52. Images of Cs_2CO_3 devices-Left: as-deposited. Right: Annealed. Some morphological effects are still visible after annealing.

We discussed as part of Year 5 the use of organophosponic acids as cathode modifiers, which are able to reduce the work function of ITO by ~2eV. These attempts to utilize phosphonic acids resulted in poor device performance and early device failure. To evaluate whether early failure was due to surface impurities deposited during the OPA treatment, a thorough cleaning process was used. Samples were fabricated using an octylphosphonic acid in THF treatment. The samples were then rinsed 5 times with clean THF. Device performance was improved over previous attempts, but was no better than devices fabricated with ITO alone.

ii. Oxidation of Calcium

An interesting observation in the HLED structure is that when no Ca injection layer is used, virtually no dark spots are created and long lifetimes are achieved. The inclusion of the Ca layer reduces the operating voltage, but leads to the formation of dark spots. The HLED anode structure slows the growth of these significantly, so that hundreds of hours of operation can be achieved. However, the ideal solution is the simultaneous reduction of operating voltage and the lack of dark spot formation. To help understand how to achieve that solution, we have investigated the behavior of the Ca layer under different oxidizing conditions, prior to the deposition of subsequent device layers. The oxidation conditions for the Ca layer were:

- Exposure to moist air for 1hr
- Exposure to an O_2 plasma at 10W for 1 min
- Exposure to a N_2 filled glove box
- Storage under high vacuum (control device)

Moist air should result in a combination of CaO and $Ca(OH)_2$. The device exposed to the oxygen plasma would only be CaO, while the device in the glove box and the device in high vacuum should not oxidize. The four devices were fabricated utilizing the standard IOLED stack. None of the first three devices (exposure to air, oxygen plasma, or glove box) showed any light emission. Only the device in which the Ca was left in high vacuum operated similarly to the previously established norm. This result suggests that there is some chemical coupling and/or doping between Ca and BCP that enables efficient electron injection, which is stable upon exposure to oxidizing environments. In contrast, oxidation of the Ca prior to BCP deposition prevents this coupling/doping mechanism. This is an intriguing result that suggests avenues for low voltage operation, while providing the good stability observed in devices without a CB layer.

iii. Discussion and Future Work

The investigations in Year 6 to demonstrate lower the operating voltage and improve device efficiency were largely unsuccessful, but did lead to several insights into the mechanism for improved stability. Each effort to lower the operating voltage and reduce the need for reactive Ca metal resulted in early device failure. This indicates that physical imperfections (roughness, particles, surface contaminants, etc.) play a major role in the overall stability and device operation efficiency. Further optimization of device design, cathode modification materials, and materials thicknesses is necessary to understand the reason for poor operating voltage and will be undertaken in the future.

Several other avenues of further study are still of interest. The doping mechanism for electron injection provides an interesting insight, and a potential route for improved results. These results show that oxidized Ca is not effective in reducing the ITO-BCP energy barrier, yet metallic Ca in contact with BCP reduces the barrier while remaining stable in an oxidizing

environment. Additional studies that seek to dope small amounts of Ca into the BCP should be performed. If effective, additional low work function dopants such as Li or Cs could be considered. In addition, the use of modified ZnO has not been fully explored.

2.3 Intellectual property

Two invention disclosures have been filed under this project at RTI. They are:
SRT-633: Hybrid organic/inorganic LEDs with surface-modified interfaces
SRT-634: Hybrid organic/inorganic LEDs with self-assembled molecular interfaces
SRT-634 was written separately because the concept of using molecular dipoles at the interface to improve charge injection came out of discussions with Greg Parsons at North Carolina State University, so the disclosure was written jointly with him.

2.4 Infrastructure development

The NC A&T and RTI facilities were well-suited for development and testing of HLED devices for environmentally stable flexible displays. However, several minor upgrades enables more rapid progress and higher quality devices. Among the upgrades, the OLED deposition system at RTI was increased from 6 to 10 sources to enable studies on multiple portions of the device (anode, cathode, and transport/emission layers) simultaneously. In addition, a second 3" RF magnetron sputter source was added to enable evaluation of doped contact layers, or simultaneous evaluation of permeation barriers and electrode layers.

3. References

1. S. Iyer and Jay Lewis: "Center of Excellence for Battlefield Capability Enhancements: Environmentally Stable Flexible Displays", [W911NF-04-1-0025] Army Research Office Interim Progress Report 1 (Report Period: 11/01/04 -7/31/05)
2. L. Wu, S. Iyer, K. Gibson, J. Li K. Matney, J. Reppert , A. M. Rao, and J. Lewis "A Study of Low-Temperature Growth of III-V Alloys for Transparent Layers " *J. Vac. Sci. Tech. B,*27, 2375-2383(2009).
3. Kenneth Lee, ARL Fellowship, Summer internship at Flexible Display Center, AZ, Final Report to ARO on "Lab View Program and 64x64 Pixel Display" , Summer 2006
4. S. Iyer and Jay Lewis: "Center of Excellence for Battlefield Capability Enhancements: Environmentally Stable Flexible Displays", [W911NF-04-1-0025] Army Research Office Interim Progress Report 3 (Report Period: 08/01/06 -7/31/07)
5. H. Han, Y. Zoo, S. Bhagat, J.S. Lewis, and T.L. Alford, *"Influence of defects and processing parameters on the properties of indium tin oxide on polyethylene naphthalate substrate"*, J. Appl. Phys., 102 (6), 63710 (2007)
6. S. Bhagat, H. Han, Y. Zoo, J. Lewis, S. Grego, K. Lee, S. Iyer, and T.L. Alford, *"Effects of deposition parameters on the electrical and mechanical properties of indium tin oxide on polyethylene naphthalate substrates deposited by sputtering"*, Thin Solid Films, 516, 4064-4069 (2008)
7. H. Han, J. W. Mayer, T. L. Alford, *"Effect of various annealing environments on electrical and optical properties of indium tin oxide on polyethylene napthalate"*, J. Appl. Phys., 99, 123711 (2006)
8. Younggun Hana, Donghwan Kim, Jun-Sik Cho, Young-Whan Beag, Seok-Keun Koh, Vladimir S. Chernysh, *"Effects of substrate treatment on the initial growth mode of indium-tin-oxide films"*, J. Appl. Phys., 97, 024910 (2005)
9. S. Iyer and Jay Lewis: "Center of Excellence for Battlefield Capability Enhancements: Environmentally Stable Flexible Displays", [W911NF-04-1-0025] Army Research Office Interim Progress Report 4 (Report Period: 08/01/07 -7/31/08)
10. A. Bowen, J. Li, J. Lewis, K. Sivaramakrishnan, T. Alford & S. Iyer, "The Properties of RF Sputtered Transparent and Conducting ZnO:F Films on Polyethylene Naphthalate Substrate", *Thin Solid Films*, 519, 1809 (2010).
11. Stanley Potoczny, "The Optical and Mechanical Properties of ZnO:F Thin Films Deposited onto Polyethylene Napthalate and Glass", M.S.E.E. Thesis, North Carolina A&T State University.
12. Adam Bowen, "The Structural and Electrical Properties of RF Sputtered ZnO:F Thin Films Deposited on Polyethylene Napthalate and Glass", M.S.E.E. Thesis, North Carolina A&T State University.
13. Elvira M. C. Fortunato, Luís M. N. Pereira Pedro M. C. Barquinha, Ana M. Botelho do Rego, Gonçalo Gonçalves, Anna Vilà, Juan R. Morante, Rodrigo F. P. Martins, "High Mobility Indium Free Amorphous Oxide Thin Film Transistors", Appl. Phys. Lett. 92, 222103 (2008).
14. Youichi Ogo, Kenji Nomura, Hiroshi Yanagi, Toshio Kamiya, Masahiro Hirano, Hideo Hosono, "Amorphous Sn–Ga–Zn–O Channel Thin-Film Transistors", Phys. Stat. Sol. (a) 205, No. 8, 1920–1924 (2008).
15. Tanina Bradley, Robert Alston, Jay Lewis, Gary Cunningham, Anil Indluru, T.L. Alford, Shanthi Iyer, "A Study of Zinc Oxide and Tin Gallium Zinc Oxide TFTs", MRS Fall Meeting, Boston, December 03, 2009.

16. A. Bowen, S. Potoczny, J. Li, K. Sivaramakrishnan, T. Alford, J. Lewis, E. W. Forsythe & S. Iyer, "The Electrical, Optical, Structural and Mechanical Properties of ZnO:F Thin Films Deposited onto Polyethylene Napthalate and Glass", selected for oral presentation at ASM/MRS NC section meeting, NCSU, Raleigh, Nov.8, 2008.
17. S. Potoczny, A. Bowen, J. Li, K. Sivaramakrishnan, T. Alford, J. Lewis, E. W. Forsythe & S. Iyer, "Properties of RF Sputtered Transparent Conducting ZnO:F Films", MRS Fall Meeting, Boston, Dec. 2, 2008.
18. A. Bowen, S. Potoczny, J. Li, K. Sivaramakrishnan, T.L. Alford, J. Lewis, E. W. Forsythe, S. Iyer, "Deposition of Transparent Conducting ZnO:F Films on PEN Substrates by RF Sputtering", 8th Annual Flexible Electronics & Display Conference, Phoenix, Feb. 2009.
19. R. Alston, T. Bradley, Jon Poe, S. Iyer, G. Cunningham, J. Lewis, and E.W. Forsythe, "OLED Degradation Testing and ZnO TFT", BCE Ann Rev Meeting, Durham, NC April 7, 2009.
20. S. Potoczny, K. Lewis, C. Prince, C. Johnson, "Backbone of the Mobile World is Getting Thin and Flexible: Automated Bend Testing System for Flexible Displays", BCE Ann Rev Meeting, Durham, April 7, 2009.
21. A. Bowen, S. Potoczny, J. Li, K. Sivaramakrishnan, T. Alford, J. Lewis, E. W. Forsythe & S. Iyer, "Deposition of Transparent Conducting ZnO:F Films on PEN Substrates by RF Sputtering", BCE Ann Rev Meeting, Durham, April 7, 2009.
22. Robert Alston, "RF-Sputtered Gallium Tin Zinc Oxide Films and Thin Film Transistors", *M.S.E.E. Thesis* 06/10
23. K. Sivaramakrishnan, A. T. Ngo, S. Iyer, and T. L. Alford, "Effect of Thermal Processing on Ag Thin Films of Varying Thickness Deposited on Zinc Oxide and Indium Tin Oxide", *Journal of Applied Physics*, 105, 063525 (2009).
24. Tanina Bradley et al. "A Study of RF Sputtered GaSnZnO TFT", manuscript in preparation.
25. Robert Alston,"A Study of Zinc Oxide and Tin Gallium Zinc Oxide TFTs", *Selected for student oral* presentation at, MRS/AVS/ASM NC Section Fall Meeting, Nov. 20, 2009, NCSU, Raleigh.
26. T. Bradley, R. Alston, J. Lewis, G. Cunningham, A. Indluru, T.L. Alford and S. Iyer, "Amorphous Gallium Tin Zinc Oxide Films and TFT Performance", 9th Annual Flexible Electronics and Displays Conference, Feb. 4, 2010, Phoenix, AZ
27. A.Bowen, J. Li, J. Lewis, K. Sivaramakrishnan, T.L. Alford, E. W. Forsythe & S. Iyer, Properties of Transparent Conducting ZnO:F Films on Glass and PEN Substrates Deposited by RF Sputtering, Poster Presentation, MRS/AVS/ASM NC Section Fall Meeting, Nov. 20, 2009, NCSU, Raleigh.
28. T. Bradley, R. Alston1, S. Iyer, and J. Lewis , G. Cunningham,"Amorphous Gallium Tin Zinc Oxide Films and TFT Performance for Flexible Electronic Implementation", Poster Presentation *at* North Carolina Nanotechnology Commercialization conference (placed 1st in the student poster presentation), Koury Convention Center, Greensboro, NC, March 31- April 1, 2010.
29. Sinelk Behane, Jazmin Clark-Harris, (LSAMP Fellows_2011), " Contact Resistance Measurements by Transfer Length Measurement", presented at 2011 NC LSAMP/RISE Joint Research Symposium, Fayettteville State Univ, 04/15/2011

Appendix A

"Display Technology" Course offered in Spring 2007 and Spring 2008 to Undergraduate Seniors and Graduate Students

NORTH CAROLINA A & T STATE UNIVERSITY
Department of Electrical and Computer Engineering

(NEW) **ELEN 685 Display Technology** ***(NEW)***

Spring 2007
T & R 4:30-5:45pm
Rm 129, McNair Hall

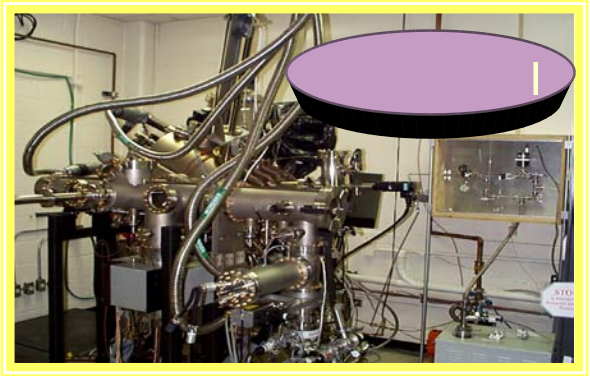
Office hours 12pm-2pm
Rm 536, McNair Hall

INSTRUCTORS: ***S.Iyer and Jay Lewis (RTI- International, Inc)***

COURSE DESCRIPTION:

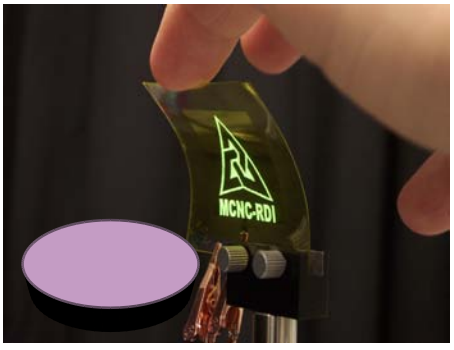
The course will provide the basic concepts on the fundamentals of light and color as the basis for understanding different display technologies at an introductory level. Fundamental aspects of different types of optical signal generation will be discussed. A review of common display technologies, typical applications of each, and some of the more interesting emerging technologies now on the horizon will be discussed. Selected standards within the display industry will be discussed in terms of the basic requirements and applications of each standard.

PREREQUISITE: ELEN 602 or consent of instructor



Course Outline:

- Overview of information displays (1 week)
- The science of light and color (1 week)
- Fundamentals of optical signal generation (1.5 weeks)
  - Photoluminescence
  - Cathodoluminescence
  - Electroluminescence
  - Liquid crystals
  - Refraction, reflection, and interference
- Transistor backplane technologies (1.5 weeks)
- Display technologies (8 weeks):
  - CRTs
  - Plasma (PDP's)
  - Liquid-crystal displays
  - Projection displays
    - LCD
    - DMD
    - LCoS
  - OLEDs
  - Field-emission displays



- Reflective displays
- Large-area displays
- Critical issues for flexible displays

- Displays standards and formats (1 week)
  - NTSC, HDTV, etc.

Participating students will take a trip to RTI (Research Triangle International) to observe real-world flexible display technology

Appendix B

L. Wu, **S. Iyer**, K. Gibson, J. Li K. Matney, J. Reppert , A. M. Rao, and J. Lewis "A Study of Low-Temperature Growth of III-V Alloys for Transparent Layers " *J. Vac. Sci. Tech. B*,27, 2375-2383(2009).

Study of low temperature growth of III-V alloys for transparent layers

L. Wu, S. Iyer,[a] J. Li, and K. Gibson
Department of Electrical and Computer Engineering, North Carolina A&T State University, Greensboro, North Carolina 27411

J. Reppert and A. M. Rao
Department of Physics and Astronomy, Clemson University, Clemson, South Carolina 29634

K. Matney
Bede Scientific Inc., Englewood, Colorado 80112

J. Lewis
RTI International Inc., Research Triangle Park, North Carolina 27709

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The authors report on the successful growth of wide band gap III-V alloy systems on glass substrates at low growth temperatures that may be suitably exploited for the realization of novel high performance and stable optoelectronic devices. A systematic investigation on the growth of GaAs, GaAlAs(N), and AlAs(N) at low temperatures ($<300\ ^\circ$C) on various substrates has been carried out to determine the effects of constituent elements of the alloy and the growth process parameters on the surface morphology and structural and optical properties of the materials. Optimized growth conditions were thus established for the successful growth of GaAlAsN polycrystalline layers with an average transmission of 80% in the visible region, with optical absorption energy >3.0 eV. The surface exhibited meandering cracks, with root mean square roughness of about 1 nm in the smooth areas between the cracks. Peaks observed in the x-ray diffraction and Raman spectra of these layers were relatively sharp in comparison to the other unoptimized quaternary layers, clearly attesting to the better quality of these layers. In addition, these layers exhibit preferential Al–N bond formation as evidenced in the corresponding Raman spectra. © *2009 American Vacuum Society.*
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I. INTRODUCTION

Low temperature growths of mixed III-V semiconductor material systems on noncrystalline materials offer potential for the realization of novel optoelectronic devices on flexible substrates by taking advantage of superior material properties and high stability of the III-V based alloy systems. Despite the expected reduction in material properties, such as mobility and doping levels compared to the epitaxial material due to both the low temperature growth and noncrystalline nature of the layers, they may still be superior to, or at least compatible with, those of competing technologies, such as organic semiconductors or amorphous silicon. These novel materials thus provide an alternate novel path for the fabrication of stable electronic devices on flexible substrates.

Among the III-V semiconductors, low temperature growth of GaAs has been the subject of extensive investigation.[1–10] These layers grown in the temperature range of 200–250 °C followed by high temperature annealing, exhibit semi-insulating properties. The high resistivity property and ultrashort carrier lifetime of the injected carriers in these layers have been successfully exploited to reduce backgating in integrated circuits[11,12] and optical switches,[13,14] respectively. However, these were grown on single crystal substrates and annealed at high temperature for rendering the material electrically active. There has been only a limited study of GaAs (Refs. 15–17) and other III-V binary compounds (Refs. 18 and 19) grown at low temperatures on unconventional substrates such as glass primarily for studying the band structure changes that occur with increased disorder in the layers. The other III-V semiconductor alloys grown at low temperatures are InGaAs,[20] GaAlAs,[21] and GaAsSb,[22] though on crystalline substrates.

We report on a systematic investigation of the low temperature ($<300\ ^\circ$C) growth of various III-V semiconductors by molecular beam epitaxial (MBE) technique, to arrive at an optimized composition for wide band gap applications with good surface morphology. The materials examined included GaAs, GaAlAs, GaAlAsN, AlAs, and AlAsN, which were grown on various substrates such as GaAs, ITO-Si, ITO-glass, and quartz glass. The effects of growth process parameters and the substrates on the surface morphology and structural and optical properties of the layers using a variety of characterization techniques, namely, x-ray diffraction (XRD), atomic force microscopy (AFM), Raman, and transmission spectra, have been presented. To the best of our knowledge, these are the first low temperature studies of III-V-N semiconductors on polycrystalline and glass substrates by any technique.

II. EXPERIMENTAL DETAILS

Low temperature growth of GaAs, GaAlAs, GaAsN, and GaAlAsN were carried out in an EPI 930 MBE system

[a]Electronic mail: iyer@ncat.edu

equipped with elemental Ga, Al, and As valved crackers with the cracker temperature at 900 °C, and an EPI Unibulb rf plasma source for N. The substrates investigated included undoped (001) GaAs, indium tin oxide (ITO) coated Si (ITO-Si), ITO coated glass (ITO-glass), and quartz glass. The growth temperature was about 250 °C, which was calibrated from the desorption of amorphous As from the surface that occurs at this temperature.[23]

The flux of the elemental sources was monitored by measuring beam equivalent pressure (BEP) using an ionization gauge. The BEP ratio of group V/III was varied from 2 to 10 for the growth of GaAs. AlAs layers were grown for two different group V/III BEP ratios of 2 and 20. The ternary and quaternary layers of AlAsN, GaAlAs, and GaAlAsN-I were grown with an As/Al ratio of 23, and an As/Ga ratio of 10 at a N BEP of 2×10^{-6} Torr. The growth of alloy composition of GaAlAsN referred to as GaAlAsN-II differed from the above quaternary layers only in the Ga pressure, which was decreased corresponding to an As/Ga ratio of 200. The optimized GaAlAsN-II layers grown with N plasma power and N BEP of 250 W and 3.2×10^{-6} Torr, respectively, are referred to as GaAlAsN. A reference sample of GaAsN was also grown for comparison. *In situ* characterization during growth was carried out utilizing a 15 KV reflection high energy electron diffraction (RHEED) gun with image acquisitions to analyze the surface reconstruction. Secondary ion mass spectroscopy (SIMS) was performed at Evans East of the Evans Analytical Group on the GaAlAsN layers.

Ex situ characterizations were performed using a Bruker AXS D8 XRD system for structural investigation, Dimension 3100 scanning probe microscope for surface morphology, and a Perkin-Elmer Lambda 900-UV-vis-NIR spectrometer with integrating sphere attachment for transmission spectral measurements. Raman measurements were also carried out on selected samples using the 514.5 nm excitation of an Ar ion laser and an ISA Triax 550 spectrometer with a typical resolution of 2.0 cm^{-1} in a backscattering geometry. The Raman signal was detected using a liquid nitrogen cooled, charge-coupled device and the peak positions were obtained from the Lorentzian fit to the data.

Layer thickness was determined using the transmission spectra, thickness profiler, and for some samples SIMS.

III. RESULTS

A. Surface morphology

1. Influence of source BEP ratio

Figures 1(a) and 1(b) are the AFM images of GaAs layers grown on GaAs substrates, exhibiting the variation in the surface morphology with As/Ga BEP ratios. For an As/Ga ratio of 2, an oriented mound pattern was observed, which shrunk with increasing BEP ratio, and eventually disappeared for a BEP ratio of 8. Root mean square (rms) roughness of the layers determined from 5×5 μm^2 images correspondingly decreased from 20 to 2 nm, consistent with brighter RHEED streaks observed for an increase in As/Ga ratio from 2 to 8, respectively. Hence subsequently, the other alloys were grown at an enhanced As/Ga ratio of 10.

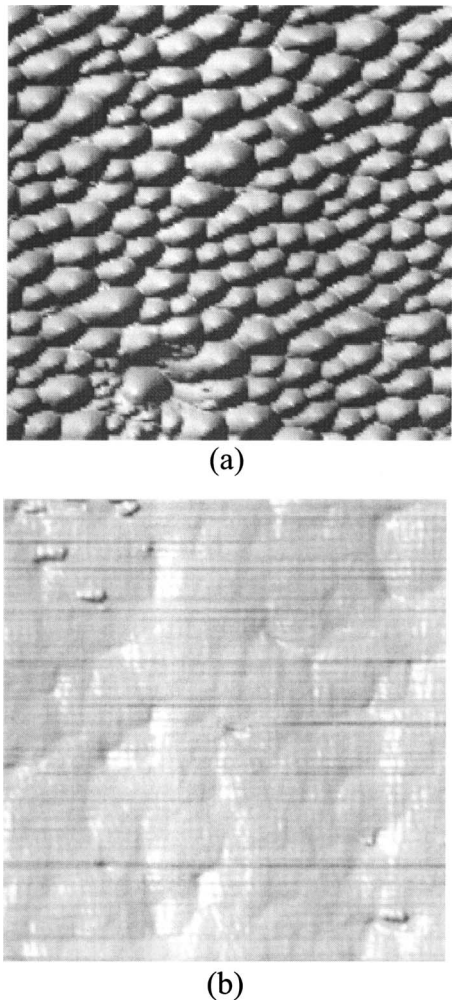

FIG. 1. 5×5 μm^2 AFM images of GaAs layers grown on GaAs at different V/III BEP ratios: (a) As/Ga=2, rms=20 nm; (b) As/Ga=8, rms=2 nm.

Figure 2 illustrates the variations in the surface morphology of GaAs with the additions of Al and N to this compound, grown on glass substrates. GaAs surface morphology displayed fine features, while AlAs surface morphology exhibited multiple facet inclinations for low As/Al BEP ratio of 2. These transformed to smoother surfaces with the formation of meandering cracks on increasing the As/Al flux ratio tenfold. This trend persisted even with the addition of N flux.

The other ternaries and quaternaries GaAsN [Fig. 2(d)], GaAlAs (not shown), and GaAlAsN [Fig. 3(d)] layers grown on glass exhibited surface morphology similar to that of GaAs, with the latter displaying oval shaped structures. The rms roughness of these layers ranged from 4 to 20 nm.

2. Influence of substrates and layer composition

Figure 3 illustrates the effect of different substrates on the surface morphology of GaAlAsN-I. The layers grown on GaAs and on ITO-Si are terraced, while the ones grown on ITO-glass and glass are rough, with the latter exhibiting oval

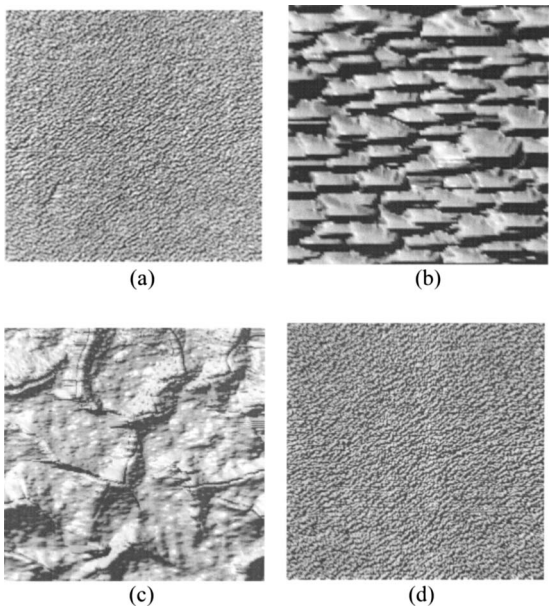

FIG. 2. 5×5 μm^2 AFM images of III-V layers grown on glass: (a) GaAs, rms=4 nm; (b) AlAs(As/Al=2), rms=20 nm; (c) AlAs (As/Al=23, 25×25 μm^2), rms=9 nm; and (d) GaAsN, rms=4 nm.

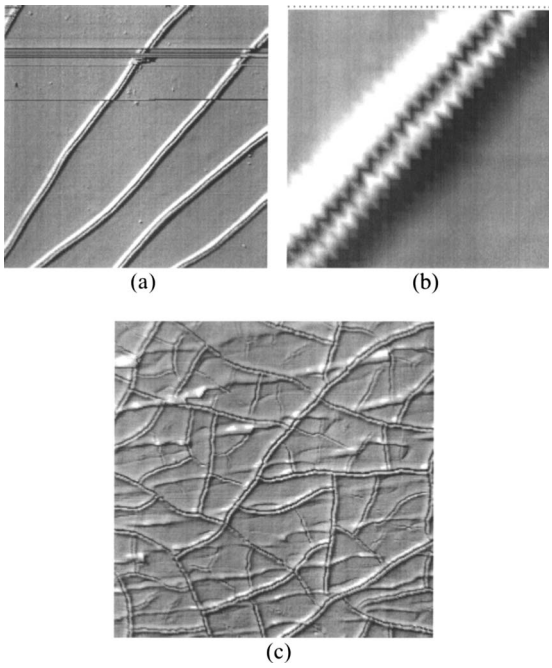

FIG. 4. AFM images of optimized GaAlAsN layers (As/Ga BEP ratio of 200) grown on (a) glass, 50×50 μm^2; (b) groves of (a), 5×5 μm^2; (c) ITO-glass, 25×25 μm^2.

shaped features. The roughness of the layers increased from 4 to 17 nm grown on GaAs, ITO-Si, ITO-glass, and glass, in that order. A similar trend was also observed on the GaAs layers (not shown) grown on the above substrates. The optimized GaAlAsN layers exhibit narrow cracks on a featureless surface [Fig. 4(a)], the cracks coverage being larger on the ITO-glass [Fig. 4(c)] in comparison to the glass substrates [Fig. 4(a)]. Figure 4(b) is the magnified image of the cracks in Fig. 4(a). The roughness of the layer [Fig. 4(a)] is about 1 nm in the smooth area and 40 nm with the cracks included.

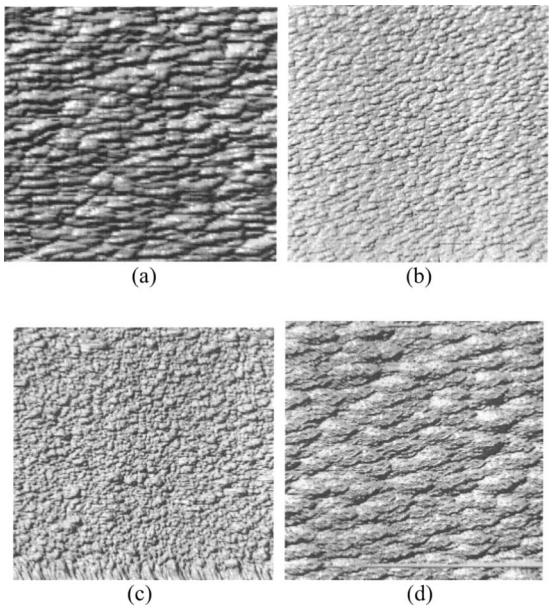

FIG. 3. 5×5 μm^2 AFM images of GaAlAsN-I layers grown on different substrates: (a) on GaAs, rms=4 nm; (b) on ITO-Si, rms=6 nm; (c) on ITO-glass, rms=13 nm; (d) on glass, rms=17 nm.

The compositions of the layers were determined using SIMS. The ratio of Ga to Al in the GaAlAsN-I layers grown with As/Ga ratio of 10, were Ga rich with Ga/Al ratio of 2.8 and N concentration of 2%. On increasing the As/Ga ratio to 200 with invariant As/Al ratio, the GaAlAsN-II layers became Al rich with Ga/Al ratio of 0.24. Due to the high O content in these layers, the anion composition could not be accurately determined and hence only group III ratios are provided. Table I summarizes the above data along with other salient growth parameters.

Adhesion of the layers were examined in a crude manner by dipping the layers in standard organic solvents, such as tricholorethylene, acetone, and methanol, followed by knife scratch and acid etching. Generally, the layer adhesion with the substrates was found to degrade in the order of GaAs, ITO-glass, and glass. Among the different layers examined that were grown on glass, AlAs and AlAsN were found to be the least adherent. The alloys with Ga and As as constituent elements such as GaAs, GaAlAs, GaAlAsN, and GaAsN displayed better adhesion.

B. X-ray diffraction

Several x-ray diffraction measurements were performed; however, only a few representative measurements are presented. The data generated were compared to the standard powder diffraction cards of GaAs (00-032-0389), AlAs (03-065-0522), and GaAlAs (00-051-1125). The x-ray diffraction spectra of GaAs, GaAlAs-I, GaAlAsN-I, and GaAlAsN

TABLE I. Summary of the layer compositions, growth and optical parameters, and surface morphology.

Samples	As/Ga ratio	Composition	Thickness (nm)	E_g from transmission plot	Simulation E_g (eV)	Simulation E_0 (eV)	rms values and surface morphology features
AlAs	As/Al =23	As/Al=1.3	350	3.4			20 nm, meandering cracks
GaAs	10		370	1.1	1.08	0.44	4 nm, smooth
GaAsN	10	$Ga_{0.490}As_{0.493}N_{0.017}$					4 nm, smooth
AlAsN	As/Al =23	As/Al=1.3, N=1 0.5%	350				
GaAlAs-I	10	Ga/Al=2.8	1024	1.7	1.92	0.43	4 nm, smooth
GaAlAsN-I	10	$Ga_{0.34}Al_{0.12}As_{0.52}N_{0.02}$	685	1.5	1.34	0.41	4 nm, oval features
GaAlAs-II	210	Ga/Al=0.24	390	2.4	1.90	0.84	160 nm, rough
GaAlAsN-II 140 W	202		257	2.4		0.80	4 nm, smooth
GaAlAsN-II 250 W	162		282	2.1	2.57	0.42	
GaAlAsN-II 400 W	210		350	2.6		0.98	17 nm, oval features
GaAlAsN 250 W	197	Ga/Al=0.24, N=1.4%	350	3	>3.0	0.52	Extremely smooth 1 nm between the cracks

samples grown on glass are shown in Fig. 5. The presence of peaks from the (111), (220), (331), and (311) orientations indicates the films are polycrystalline. The layers grown on GaAs substrates exhibited only (00n) peaks (not displayed), indicative of a single crystal nature of the layer. The lattice parameters were found to vary with the diffraction planes (peak positions are shifted from their ideal locations), indicating a noncubic lattice. Grain size analyses on these layers were carried out using the Scherer equation from the full width at half maxima (FWHM) of the x-ray diffraction peaks averaged over several planes. The grain size was found to decrease in the order of GaAsN (180 Å), GaAlAs (140 Å), GaAlAsN (70–90 Å), AlAs (55 Å), and AlAsN (40 Å) layers, suggesting a smaller grain size in Al rich alloy layers and Al plus N mixed alloy layers. Grain size of GaAlAsN layers grown on ITO-Si was estimated to be about 226 Å, somewhat higher than those grown on glass substrates.

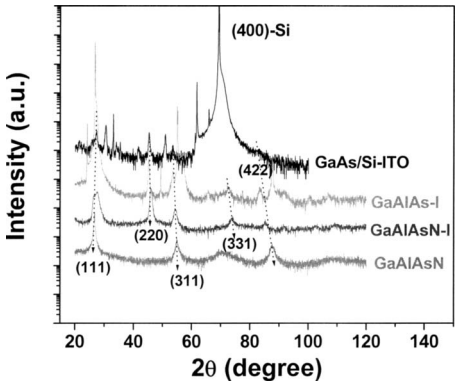

FIG. 5. X-ray diffraction scan curves of (a) GaAlAsN-I and optimized GaAlAsN layers grown on glass and GaAs grown on ITO-Si and (b) AlAsN and AlAs layers grown on glass.

C. Transmission spectra

Figures 6(a) and 6(b) exhibit the transmission spectra of GaAs, AlAs, GaAlAs-I, GaAlAs-II and GaAlAsN-I layers grown on glass. The transmission edge was taken to be at the wavelength, where the transmission of the layers drops to 20%. It varied from 1.11 to 3.41 eV for GaAs and AlAs, respectively. The transmission edges of GaAlAs-I and GaAlAsN-I with As/Ga ratio of 10 fell in the intermediate region close to 1.73 and 1.49 eV [Fig. 6(b)], respectively, which blueshifted to 2.38 and 2.64 eV, respectively, with an increase in As/Ga BEP ratio of 200.

As improved surface morphology and a better transmission spectra were obtained for the GaAlAsN-II layers, these layers were further fine tuned for N plasma power and flux. The results are shown in Fig. 7 for the layers grown on glass. For an intermediate plasma power of 250 W, the transmission edge was found to be somewhat sharp, occurring at 2.12 eV. With the N power set at this optimized power, transmission edge was further blueshifted to 3.01 eV with an increase in N pressure from 2×10^{-6} to 3.2×10^{-6} Torr, the highest N pressure that we can get in our system. The layer grown at this optimized power and N pressure of 3.2

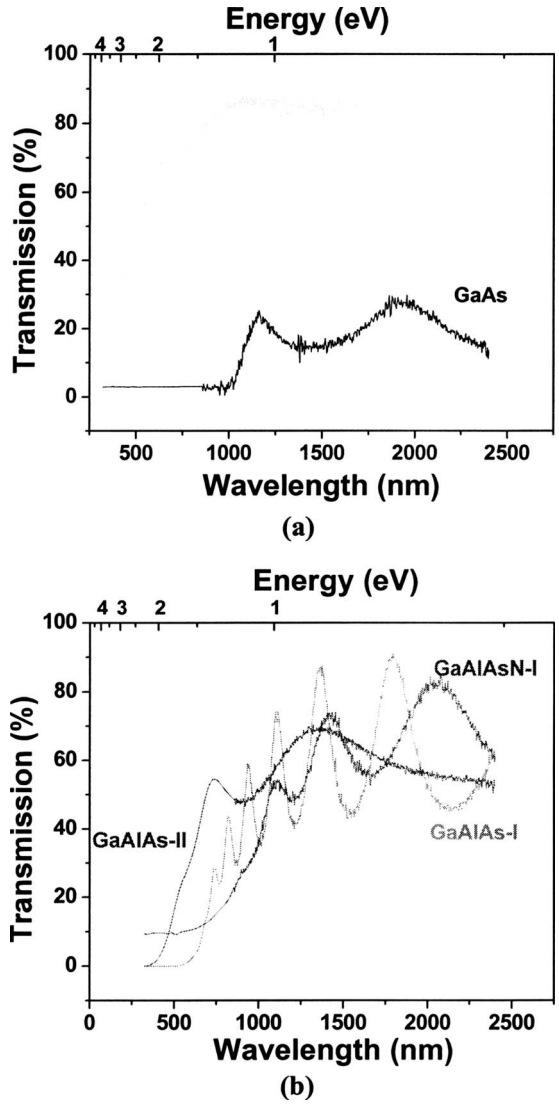

FIG. 6. Transmission spectra of layers grown on glass: (a) GaAs and AlAs layers, (b) GaAlAs-I, GaAlAsN-I layers at an As/Ga BEP ratio of about 10 and GaAlAs-II layers at an As/Ga BEP ratio of about 200.

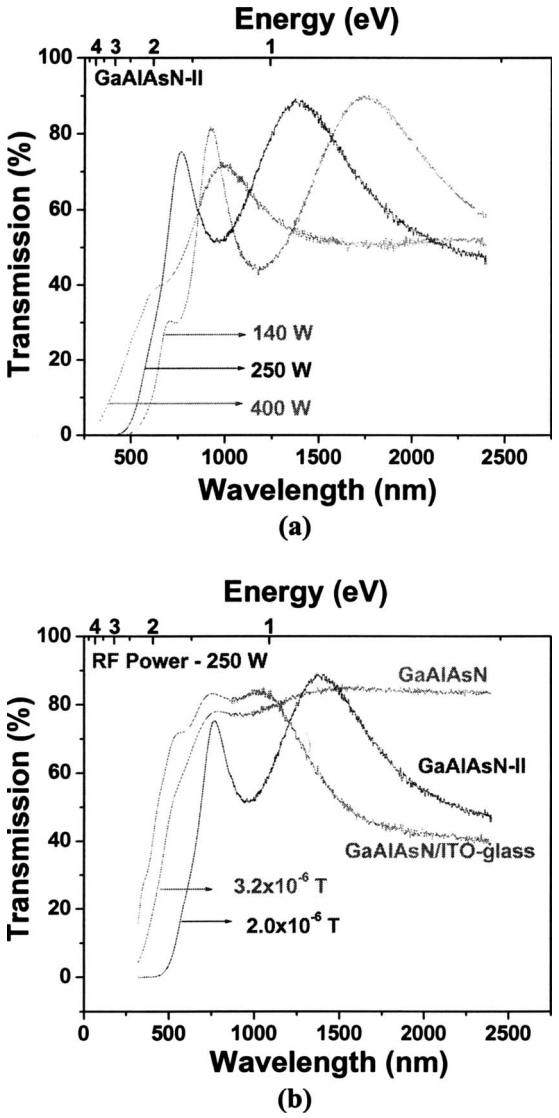

FIG. 7. Effects of (a) N plasma power and (b) N flux on the transmission spectra of GaAlAsN-II layers grown on glass. Also spectra of optimized GaAlAsN on ITO-glass is displayed for comparison.

$\times 10^{-6}$ Torr on ITO-glass had excellent transmission characteristics almost closely replicating the ITO-glass spectra, as shown in Fig. 7(b).

Figures 8(a) and 8(b) display the corresponding absorption spectra. It is to be noted that the actual values of the absorption coefficient, α, have an uncertainity of $\pm 20\%$ determined from the repeated transmission and reflection runs. However, these curves provide an accurate guideline for the trends observed with varying composition. Four distinct regions can be distinguished in the absorption curve plot of the ternary and quaternary alloys [Fig. 8(c)]: (a) band to band absorption given by $\alpha \propto (h\nu - E_g)^{1/2}$, where E_g and $h\nu$ represent the band gap and incident photon energy, respectively, (b) the Urbach edge absorption regions corresponding to the exponential variation in α on energy close to the band gap as given by $\alpha = \alpha_g \exp[(h\nu - E_g)/E_0]$, where E_0 is the Urbach parameter, (c) another weaker exponential functional dependence corresponding to the weak absorption tail over a broad energy range, and finally (d) free carrier absorption where α increases with decrease in energy. It may be observed that the absorption curve of GaAs is sharp and, in the ternary and quaternary layers, the spectra labeled as "II" corresponding to increased As/Ga ratio are smeared. Band to band absorption could not be fitted in AlAs, being an indirect gap, and in a few of the GaAlAsN-II samples. The value of E_g that provided a good fit to the experimental data near the band gap and corresponding Urbach parameters are listed in Table I.

D. Raman spectra

Room temperature Raman spectra of GaAlAsN-I and optimized GaAlAsN layers, along with the reference layers of GaAsN and AlAsN grown on glass by molecular beam epitaxy, are shown in Fig. 9. The Raman spectra of the reference layer GaAsN contain the normal GaAs TO and LO modes of 270 and 294 cm^{-1}, respectively.[2] AlAsN layers exhibited a

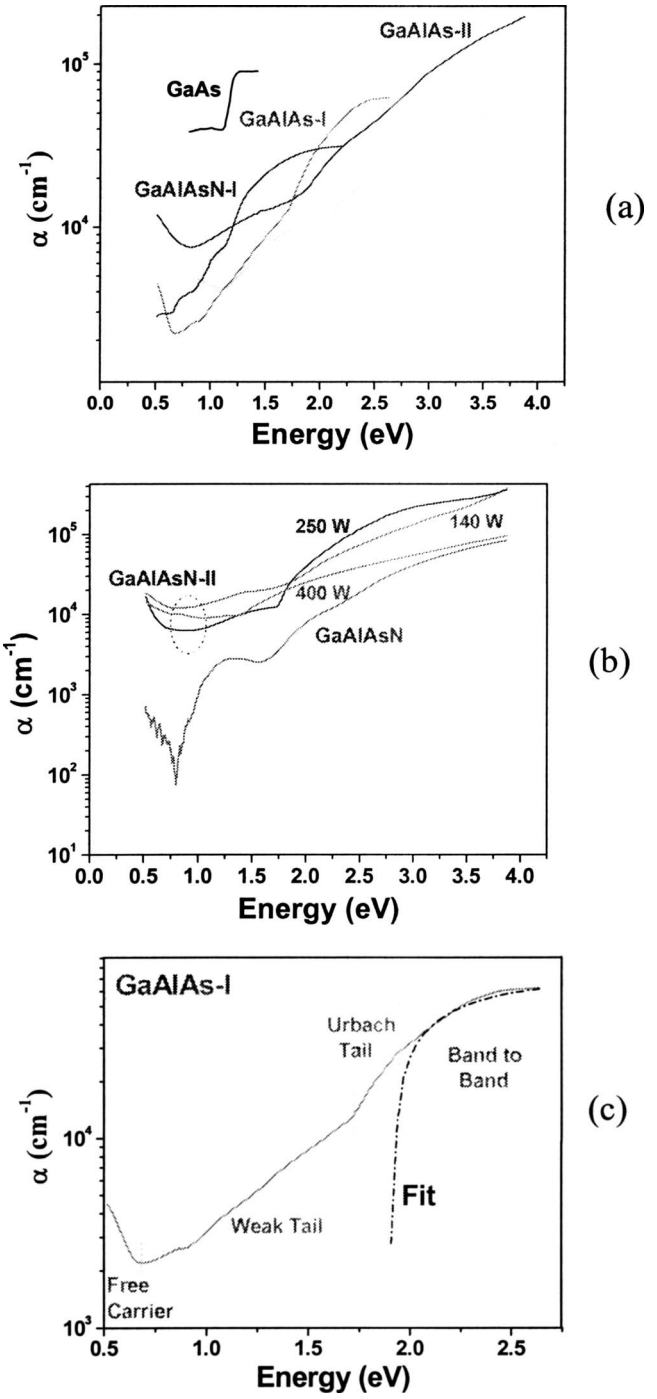

FIG. 8. (a) Energetic dependence of the absorption coefficient for GaAs, AlAs, GaAlAs-I, GaAlAs-II, GaAlAsN-I layers on glass. (b) Variation in the absorption coefficient of GaAlAsN-II for different plasma powers and for the optimized GaAlAsN layer. (c) Absorption spectrum of GaAlAs-I with four distinct regions of absorption identified. Theoretical fit of the direct band edge is superimposed on the experimental data.

dominant peak at 470 cm^{-1} due to Al–N related modes and a broad peak at 254 cm^{-1}, assigned in the literature to the AlAs LO_2 mode.[24] Raman spectra are broad for GaAlAsN-I layers [Fig. 9(c)], exhibiting a peak at 273 cm^{-1} with a shoulder labeled as AL (acoustic local) at the lower frequency side and a peak at 370 cm^{-1}. GaAlAsN layers, in contrast, exhibit

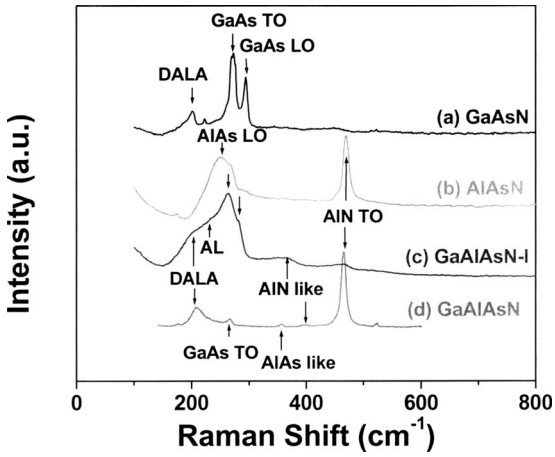

FIG. 9. Room temperature Raman spectra of (a) GaAsN, (b) AlAsN, (c) GaAlAsN-I, and (d) optimized GaAlAsN layers grown on glass.

sharper peaks and are dominated by the optical mode at 465 cm^{-1} [Fig. 9(d)]. The other observed peaks, at 400, 358, and 266 cm^{-1}, are assigned to higher order AlN like peaks, AlAs-like LO_2 phonon mode,[24] and GaAs TO mode,[25] respectively. The broad peak at 209 cm^{-1} was also reported by Kawamura *et al.*[25] for GaAlAs and have been attributed to disorder activated longitudinal acoustic mode due to the As crystalline phase present on the surface of the sample, when grown at low temperatures.[26]

IV. DISCUSSIONS

The surface morphology of GaAs transforms from mounds to a smooth surface, while in AlAs layers a faceted surface changes to the formation of cracks, with increase in group V/III BEP ratio. Also the overall surface roughness is decreased in both cases for higher group V/III ratios. Among the ternary alloys, the surface morphologies of the GaAlAs and GaAsN layers are somewhat analogous to that of GaAs, while AlAsN reveal crack formation similar to AlAs layers. In the quaternary GaAlAsN-I layers small mounds superimposed on the fine features are transformed to smooth surface with meandering cracks, with increase in the As/Ga ratio. These observations clearly indicate that high As flux on the surface significantly improves the surface morphology, while with increasing Al content the surface becomes rougher, faceted, and more prone to crack formation, and finally introduction of N leads to fine features.

The surface morphology differences observed in these alloys can be qualitatively explained in terms of the initial stages of growth as follows. The size and height of the stable island at the inception depend on the surface energy difference between the alloys/substrate and the cohesive energy of the alloys. The decreasing trend in the grain size along with a corresponding increase in the surface roughness, as the alloy layer grown on glass gets richer in Al and N constituents, can be attributed to the stronger bonding between the two constituent elements (discussed later) and higher surface energy associated with Al containing system.[27] As a result, island growth is likely to dominate over the lateral growth.

However, with increase in As/Ga ratio, the excess As atoms accumulated on the surface act as surfactant,[28] passivate the surface, and decrease the surface diffusion energy barrier resulting in an enhanced migration of group III adatom. The coalescence mechanism of the nuclei and hence the growth kinetics are altered, leading to smoother surface. This is consistent with the comparatively smoother morphology achieved in layers with higher As/Ga ratio, particularly in GaAlAsN-II and GaAlAsN layers. Further, the observed surface morphology differences in AlAs and GaAs based alloys not only stem from the differences in surface energy between the Al based and Ga based alloys, with the former possessing higher energy,[27] but also because Al has a lower, as well as anisotropic diffusivity, in comparison to Ga.[29,30] Hence, the growth is more likely to be surface energy controlled with inclinations of lower surface energies stabilizing the growth. Furthermore, the lattice dilation due to the incorporation of excess As in the layer[7,31] in conjunction with the high thermal expansion coefficient associated with Al containing alloys leads to large stress built up in the layer during the postgrowth cooling, resulting in the formation of cracks. Addition of N only alters the fine features in all the alloys. Thus, both Ga and As smoothen the surface, while Al contributes to the stress component and N alters the fine features on the surface. This inference qualitatively explains the differences observed in the adhesion between Ga- and Al-rich alloys,[32] with the latter exhibiting poorer adhesion. The roughness increases (see Fig. 4) for a given constituent layer grown on various substrates in the order of lower degree of crystallinity–GaAs, ITO-Si, ITO-glass, and glass. From our limited study, the grain size is decreased for layers grown on glass as compared to layers grown on ITO. As the surface energy of glass is higher than ITO,[33,34] the smaller grain size observed on glass is speculated to be the result of the differences in the interaction energies between the layer and the substrates.

All the layers were largely polycrystalline as evidenced by the presence of peaks from several diffraction planes, which is also consistent with the semicircular rings observed in the *in situ* RHEED pattern (not shown). Not every diffraction plane is present, indicative of some residual preferred orientation in the films. The lattice parameters of all the alloys with Ga as one of the constituent element are close to that of GaAs. However, there is a variation in the peak positions suggesting a noncubic lattice. This distorted lattice is presumably due to the large density of point defects, which is a characteristic of LT-GaAs layers.[35] The lattice parameters of AlAs and AlAsN could not be matched to any known compound and the peaks were considerably broad, consistent with the high surface roughness exhibited by these layers. The FWHM of the optimized GaAlAsN XRD peaks were found to be the narrowest, consistent with the sharp and rich spectral features of the corresponding Raman spectra as well as smooth surface topography exhibited by these layers.

The values of the transmission edge and absorption edges, as listed in Table I, were in good agreement for most of the samples and the blueshifts observed with higher Al/Ga ratio in both GaAlAs and GaAlAsN were also consistent. The absorption spectrum of GaAs was found to be the sharpest, although the absorption edge occurs at much lower energy than for the crystalline GaAs. Similar redshift in the absorption edge grown at such low temperatures by MBE has been reported by Azevedo *et al.*[17] The α values on GaAs layers are comparable, although the E_0 values are higher in our layers with lower E_g. As E_0 provides a measure of the disorder associated with either or a combination of thermal, structural, and compositional disorders, higher values of E_0 determined in our GaAs samples are representative of increased disorder leading to band tail states extending deeper in the band gap, thereby reducing the band gap lower than those reported by Azevedo *et al.*[17] The E_0 values are much larger in the ternary and quaternary layers and fell in the range of 0.40–1.00 eV. They were found to be influenced strongly by the III-V flux (Al/Ga, As/Ga) ratio and N plasma power. Higher values of E_0 correspond to a higher (Al/Ga, As/Ga) ratio. Similar large values in III-V material system have been reported by Han *et al.*[36] in $In_{0.13}Ga_{0.87}N$ epilayers grown by metal-organic chemical vapor deposition (MOCVD) and have been attributed to compositional disorder arising from miscibility gap. The anomolously large values of E_0 exhibited by our ternary and quaternary layers may thus be attributed to the well known large compositional disorder associated with dilute nitride alloys,[37] in combination with the structural disorder arising from the low temperature growth. The determination of E_g becomes a challenge on these samples due to the deep protrusion of the Urbach edge in the band gap. However, the E_0 value could be reduced to 0.49 eV, as in the optimized GaAlAsN layers, by tuning the N flux and plasma power. This shows that the tail states can be localized by tailoring the growth parameters resulting in the blueshift of the band gap and decreased optical absorption.

The Raman spectra of these layers [Fig. 9(d)] exhibit a dominant vibrational optical mode at 465 cm^{-1}, which can be attributed to either Ga–N like and/or Al–N related modes. The contribution of the latter appears to be more dominant due to a similar sharp peak observed at 470 cm^{-1} in the AlAsN sample [Fig. 9(b)] and the absence of a peak in GaAsN grown under analogous BEP ratios and growth conditions. The observed shift from 470 to 465 cm^{-1} could most probably be a result of the local strain around N. For the optimized GaAlAsN layers, the bonding of Al to N is favored over Ga to N (Ref. 24) due to the larger cohesive energy of 2.88 eV. Increasing the Ga content in the GaAlAsN-1 system (As/Ga=10) results in vanishing of the AlN related peak at 470 cm^{-1} and appearance of a new peak at 370 cm^{-1}. This behavior is speculated to stem from the strain induced by the statistical distribution of $Al_nGa_{4-n}N$ (n=0–4) (Ref. 38) in the GaAlAs matrix, caused by the large differences in the lattice constant and force constants of AlN and GaN. Thus, the bond states of N atoms in the $Al_nGa_{4-n}N$ unit are largely determined by the vibrational mode of AlN complex at 370 cm^{-1}.[38] This is consistent with the reports by Geppert *et al.*[24] on dilute GaAlAsN system

where only Al–N vibrational mode was observed even though they were grown at a higher growth temperature.

The Raman spectra for GaAlAsN-I layers corresponding to the lower As/Ga ratio exhibit only a few peaks, which are also broad. This is associated with inferior sample crystalline quality in comparison to the optimized sample, consistent with the x-ray data presented earlier. The broad peak at 273 cm^{-1} is the GaAs TO mode shifted by a few wave numbers (cm^{-1}) relative to the optimized layer due to strain effects. We speculate the shoulder AL at the lower frequency side of this peak [Fig. 9(c)] to be caused by the local acoustic mode arising from the substitution of Al on Ga sites.[25] This conclusion has been drawn based on the broad peak observed at 254 cm^{-1} in AlAsN layers [Fig. 9(b)], assigned in the literature to the AlAs LO_2 mode.[25]

All these characteristics indicate that excess As (As/Ga BEP ratio of 200), as evident from the Raman peak corresponding to the crystalline phase, acts as a surfactant and, in combination with the Ga flux, provides a smooth growth front. But increasing Ga content redshifts the absorption edge. This can be offset by the introduction of Al and an increased Al/Ga ratio, which blueshifts the absorption edge to improve the transmission range in the visible region. However, improved Al content leads to cracking, attributed to both the anisotropic diffusion of Al as well as a high thermal expansion coefficient associated with Al alloys. Hence, the GaAlAs-II layer is more disordered exhibiting a broad optical absorption tail. Addition of the fourth component N to the alloy and by appropriately tuning the N plasma, the absorption edge can be shifted to higher photon energy, which has been correlated to the stronger bonding of AlN and localized states in the band gap. For this optimized GaAlAsN composition, the x-ray and Raman spectra display sharp peaks and the surface morphology is smooth, although the layer surface becomes prone to cracking due to the stress built up in the layers caused by the large difference in AlN and GaN bond lengths. Thus, the data clearly indicate that, by appropriately tailoring the constituents of the alloy, one can achieve a wide band gap III-V alloy layer of GaAlAsN of good crystal quality and surface morphology on noncrystalline substrates. The electrical properties of these layers must be investigated to evaluate their promise for flexible electronics applications.

V. CONCLUSIONS

In conclusion, the low temperature grown layers of mixed III-V alloys on noncrystalline substrates exhibit polycrystalline structure. It has been found that the high As/group III BEP ratio and Ga improves the surface morphology significantly, while Al roughens the surface and increases the disorder in the layers, but blueshifts the transmission edge. The addition of N provides another degree of freedom that allows further tuning of all the properties of the layers. By appropriately tuning the N plasma the optimized GaAlAsN quaternary layers were successfully grown on glass and exhibited an average transmission better than 80% in the visible region with rms surface roughness of about 1 nm. The optical absorption edge blueshifted with the reduction in the width of the band tail states in the band gap. The good quality of the layers and dominance of AlN bonding on these layers were evident by the presence of sharp peaks and an AlN related peak at 465 cm^{-1}, respectively, in the corresponding Raman spectra.

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[1] J. N. Miller and T. S. Low, J. Cryst. Growth **111**, 30 (1991).
[2] T. A. Gant, H. Shen, J. R. Flemish, L. Fotiadis, and M. Dutta, Appl. Phys. Lett. **60**, 1453 (1992).
[3] D. Look, Thin Solid Films **231**, 61 (1993).
[4] R. E. Pritchard, S. A. McQuaid, L. Hart, R. C. Newman, J. Mtikinen, H. J. von Bardeleben, and M. Missous, J. Appl. Phys. **78**, 2411 (1995).
[5] M. Lagadas, Z. Hatzopoulos, K. Tsagaraki, M. Calamiotou, C. Lioutas, and A. Christou, J. Appl. Phys. **80**, 4377 (1996).
[6] M. Missous, Mater. Sci. Eng., B **44**, 304 (1997).
[7] M. Luysberg, H. Sohn, A. Prasad, P. Specht, Z. Liliental-Weber, E. R. Weber, J. Gebauer, and R. Krause-Rehberg, J. Appl. Phys. **83**, 561 (1998).
[8] J. Herfort, V. V. Prebrazhnskii, N. Boukos, G. Apostolopoulos, and K. H. Ploog, Physica E (Amsterdam) **13**, 1190 (2002).
[9] R. Enrique Viturro, M. R. Melloch, and J. M. Woodall, Appl. Phys. Lett. **60**, 3007 (1992).
[10] D. Youn *et al.*, J. Appl. Phys. **103**, 123528 (2008).
[11] F. W. Smith, A. R. Calawa, C. Chen, M. J. Manfra, and L. J. Mahoney, IEEE Electron Device Lett. **9**, 77 (1988).
[12] D. B. Janes *et al.*, J. Vac. Sci. Technol. B **17**, 1773 (1999).
[13] G. C. Loata, T. Löffler, and H. G. Roskos, Appl. Phys. Lett. **90**, 052101 (2007).
[14] Y. C. Shen *et al.*, Appl. Phys. Lett. **85**, 164 (2004).
[15] H. M. Heiliger, M. Vossebürger, H. G. Roskos, H. Kurz, R. Hey, and K. Ploog, Appl. Phys. Lett. **69**, 2903 (1996).
[16] M. Imaizumi, M. Adachi, Y. Fujii, Y. Hayashi, T. Soga, T. Jimbo, and M. Umeno, J. Cryst. Growth **221**, 688 (2000).
[17] G. de M. Azevedo, J. H. Dias da Silva, and E. Avendano, Nucl. Instrum. Methods Phys. Res. B **238**, 329 (2005).
[18] W. Eckenbach, W. Fuhs, and J. Stuke, J. Non-Cryst. Solids **5**, 264 (1971).
[19] J. Stuke and G. Zimmerer, Phys. Status Solidi B **49**, 513 (1972).
[20] J. M. Kim, Y. T. Lee, J. D. Song, and J. H. Kim, J. Cryst. Growth **265**, 8 (2004).
[21] M. Missous, Microelectron. J. **27**, 393 (1996).
[22] J. Sigmund, C. Sydlo, H. L. Hartnagel, N. Benker, H. Fuess, F. Rutz, T. Kleine-Ostmann, and M. Koch, Appl. Phys. Lett. **87**, 252103 (2005).
[23] V. V. Preobrazhenskii, M. A. Putyato, and B. R. Semyagin, Semiconductors **36**, 837 (2002).
[24] T. Geppert, J. Wagner, K. Kohler, P. Ganser, and M. Maier, Appl. Phys. Lett. **80**, 2081 (2002).
[25] H. Kawamura, R. Tsu, and L. Esaki, Phys. Rev. Lett. **29**, 1397 (1972).
[26] G. Apostolopoulos, N. Boukos, J. Herfort, A. Travlos, and K. H. Ploog, Mater. Sci. Eng., B **88**, 205 (2002).
[27] W. Liu, W. T. Zheng, and Q. Jiang, Phys. Rev. B **75**, 235322 (2007).
[28] A. Shen, H. Ohno, Y. Horikoshi, S. P. Guo, Y. Ohno, and F. Matsukura, Appl. Surf. Sci. **130–132**, 382 (1998).
[29] B. Brar and D. Leonard, Appl. Phys. Lett. **66**, 463 (1995).
[30] S. J. Brown, M. P. Grimshaw, D. A. Ritchie, and G. A. C. Jones, Appl. Phys. Lett. **69**, 1468 (1996).
[31] M. Kaminska, Z. Liliental-Weber, E. R. Weber, T. George, J. B. Kortright, F. W. Smith, B.-Y. Tsaur, and A. R. Calawa, Appl. Phys. Lett. **54**, 1881 (1989).
[32] Y. Liu and Q. Zhao, Biophys. Chem. **117**, 39 (2005).

[33]J. S. Kim, R. H. Friend, and F. Cacialli, Synth. Met. **111–112**, 369 (2000).
[34]J. J. Stephens and K. Scott Well, *Brazing and Soldering: Proceeding of the Third International Brazing and Soldering Conference* (ASM, Metals Park, OH, 2006), p. 113.
[35]T. E. M. Staab, R. M. Nieminenb, M. Luysbergc, J. Gebauerd, and Th. Frauenheime, Physica B **340–342**, 293 (2003).
[36]B. Han, B. W. Wessels, and M. P. Ulmer, J. Appl. Phys. **99**, 084312 (2006).
[37]J. Li, S. Iyer, S. Bharatan, L. Wu, K. Nunna, and W. Collis, J. Appl. Phys. **98**, 013703 (2005).
[38]K. Yamamoto, M. Uchida, A. Yamamoto, A. Masuda, and A. Hashimoto, Phys. Status Solidi B **234**, 915 (2002).

Appendix C

A. Bowen, J. Li, J. Lewis, K. Sivaramakrishnan, T. Alford & **S. Iyer,** "The Properties of RF Sputtered Transparent and Conducting ZnO:F Films on Polyethylene Naphthalate Substrate", *Thin Solid Films*, 519, 1809 (2010).

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The properties of radio frequency sputtered transparent and conducting ZnO:F films on polyethylene naphthalate substrate

A. Bowen [a,*], J. Li [a], J. Lewis [b], K. Sivaramakrishnan [c], T.L. Alford [c], S. Iyer [a]

[a] Department of Electrical and Computer Engineering, North Carolina Agricultural and Technical State University, Greensboro, NC 27411, USA
[b] RTI International Inc., RTP, NC 27709, USA
[c] Department of Chemical and Materials Engineering and Flexible Display Center, Arizona State University, Tempe, Arizona 85287, USA

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ABSTRACT

We report on the properties of ZnO:F films deposited by RF sputtering on polyethylene naphthalate (PEN) substrates and compared them with films deposited on glass. Detailed and systematic investigations of various properties of films were deposited on PEN substrates were carried out as functions of thickness and annealing ambient. The films were deposited at room temperature and annealed at 150 °C in either Ar or 7% H_2/Ar ambients. These films exhibited carrier concentrations between 2×10^{18}/cm^3 and 9.5×10^{19}/cm^3, mobility between 3 and 11 cm^2/V-s, and resistivity between 10^{-1} and 10^{-2} Ω-cm. Hall mobility variation with concentration has been explained assuming ionized impurity and lattice scattering to be the dominant mechanisms. The transmission of the films varied from 68 to 80% with increasing thickness and the absorption edge was limited by the absorption of the PEN substrate. The mechanical flexibility of the films was measured in terms of its critical radius of bending which was determined from the onset of a sharp increase in electrical resistance. The critical radius varied between 6.5 and 17 mm for film thicknesses varying from 20 to 200 nm. The thickness dependence of critical strain and critical radius can be explained by Griffith defect theory.

1. Introduction

Currently, there is a considerable research interest in finding an alternative transparent and conducting oxide (TCO) material system for the presently used indium tin oxide. Amongst these alternatives, ZnO and its alloy films are the most extensively investigated system. With the increasing cost of In material systems, ZnO provides a less expensive solution. Further, ZnO allows lower deposition temperatures and is more stable in activated hydrogen environments than other TCOs [1,2].

The current trend is towards the use of TCO coatings deposited onto flexible polymer substrates for electronic and opto-electronic device applications. With advantages including reduced weight, increased ruggedness, increased flexibility and portability, flexible polymers offer great opportunities for the next generation of devices, which conventional and rigid substrates cannot provide.

There are numerous reports [3–6] on the electrical, optical, and mechanical properties of Al and Ga doped ZnO deposited on polymer substrates. In this work, we investigated F-doped ZnO films deposited at room temperature with subsequent annealing at 150 °C. This temperature is below the polymer temperature threshold. Fluorine was chosen due to the high figure of merit [7] exhibited when used as a ZnO dopant. The figure of merit for a transparent conductive oxide is defined as the ratio of electrical conductivity to the optical absorption coefficient of the film [7]. Further, F-doped tin oxide films have shown potential for work function modulation [8]. There have been recent studies [9–14] on F-doped ZnO films, predominantly synthesized by chemical spray pyrolysis. Shinde et al. [13] reported a resistivity of 6.63×10^{-4} Ω-cm, with mobility as high as 87.2 cm^2/V-s, on films deposited at 400 °C with 15 at.% doping and annealed in an atmospheric ambient for 2 h at 200 °C. In recent years RF sputtered F-doped ZnO films have been reported [14,15]. Tsai et al. [14] reported the effects of annealing on the properties of F-doped films prepared from a ZnF_2 target and found that 500 °C vacuum annealing yielded a carrier concentration in the 10^{21}/cm^3 range with mobility approximately 4.8 cm^2/V-s. Yoon et al. [15] carried out a detailed study on the properties as a function of doping concentration for films deposited using a ZnO target in CF_4 containing gas mixtures [15]. They reported carrier concentrations in the low 10^{20}/cm^3 range with mobilities in the range of 40 cm^2/V-s on room temperature deposited films annealed at 300 °C in vacuum. Yoon et at. [15] also reported F-doped ZnO films deposited at an elevated temperature of 150 °C had

* Corresponding author.
E-mail address: bowen.adam@gmail.com (A. Bowen).

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significantly lower fluorine content and exhibited a lower carrier concentration of $1.7\times10^{19}/cm^3$ and a mobility of 4.7 $cm^2/V\text{-}s$.

In this work, we report on the effect of thickness and annealing ambient on the surface morphology, structural, optical, electrical and mechanical properties of room temperature RF magnetron sputtered ZnO:F films on polyethylene naphthalate (PEN) substrates.

2. Experimental details

ZnO containing 2 wt.%F was used as the sputtering target. The 100 mm target was pre-sputtered in Ar/O_2 ambient for 10 min prior to each deposition and the substrates were plasma etched in the deposition chamber at 5 Pa in Ar at a constant plasma power of 10 W. Argon was used as the sputter enable gas and the process pressure was 0.7 Pa for all depositions. Depositions were carried out at room temperature at a constant power of 120 W on 200 μm thick DuPont Teonex® Q65 PEN substrates. These PEN substrates were specifically heat-stabilized for improved thermal and mechanical properties. For instance, these PEN substrates are rated for processing temperatures of 180–220 °C which are higher than conventional PEN. Further, these exhibit a lower shrinkage, Young's Modulus, and coefficient of thermal expansion (CTE) than that of untreated PEN substrates [16]. Hence, a post-deposition annealing temperature of 150 °C was chosen for our ZnO:F films. Annealing of the samples was performed in the sputtering chamber under different ambients of Ar and 7% H_2/Ar at 150 °C for periods of 1 h.

Films deposited on silicon substrates from each run were used to confirm thickness measurements through spectral ellipsometry. Surface morphology was examined using a NanoScope III Dimension 3100 atomic force microscopy (AFM) system, run in tapping mode using a RTESP Si tip from Digital Instruments. The tip has an anisotropic geometry with a height of 15 μm and radius of 8 nm. X-ray diffraction (XRD) was performed using a Bruker AXS D8 Discover Series diffractometer with Cu Kα radiation ($\lambda = 0.15406$ nm) and a 0.2 mm slit to analyze sample crystallinity.

Zn and O concentrations were determined using the elastic nuclear resonance technique in Rutherford backscattering geometry (RBS). Quantitative information about light element concentrations is obtainable using resonance in an energy regime in which the scattering cross-section [17] varies less rapidly and may more accurately predict the actual composition than standard RBS. In this case the oxygen resonance $^{16}0(\alpha,\alpha)^{16}0$ was used which occurs at an energy of 3.04 MeV [18]. The Zn and O compositions are determined initially using a 3.04 MeV beam that provided an enhanced O signal. The Zn composition was then further corroborated using a 2.0 MeV beam energy in the conventional Rutherford cross-section. The ZnO:F films were tilted to 65° to increase the depth resolution. The RBS data was analyzed using RUMP computer-simulation program [19]. This approach provides sensitivity to concentrations on the order of 1.0–0.5 ± 0.1 at.%. Secondary ion mass spectroscopy (SIMS) analysis was used to verify the presence of F in the films; however, it could not be quantified due to a lack of a known reference.

Electrical measurements were performed using a Varian Hall Effect measurement system, using magnetic fields of 0.8 T and the van der Pauw configuration. Bend testing of the samples was carried out using a collapsing radius system built in-house [20] where the film was held between two flat parallel fixtures containing electrical connections. One of the sample holders is fixed while the other holder is controlled by a linear actuator. The experiments were performed with samples typically 7.5 cm long and 0.5 cm wide with the film on the outer bend surface of PEN substrate such that it undergoes tensile strain. The distance between the plates is determined by the length of the sample such that the sample is loaded in a curved shape which is sufficiently larger than the failure criterion under bend testing. The plates are then gradually collapsed from the initial distance L between the two plates to the desired radius r by moving the mobile fixture, where $r = L/2$. It should be noted that the sample curvature is non-uniform, and that this definition of r is an approximation.

3. Results

3.1. Surface morphology

AFM images were taken of films deposited on both PEN and glass substrates, as functions of thickness and annealing ambient. Table 1 displays the root mean square (RMS) roughness values for films on PEN and glass with different film thicknesses and annealing ambients measured on a 2 μm×2 μm image. It is to be noted that the bare PEN substrates displayed an initial roughness of about 2.1 nm. Fig. 1(a) shows an AFM image of an as-deposited 146 nm ZnO:F film on a PEN substrate, which exhibits a non-uniform grain distribution with ~50 nm protrusions from an otherwise, smooth surface morphology, corresponding to a RMS roughness value of 9.7 nm. Fig. 1(b)–(d) displays AFM images of the Ar annealed ZnO:F films of varying thickness deposited on a PEN substrate. The 49 nm thick Ar annealed film exhibited uniform grain structure, densely packed and smooth surface morphology. With increasing thickness, the AFM images show surface roughness increases with non-uniform distribution of grains of various sizes. Fig. 1(e)–(f) displays the surface morphology of 7% H_2/Ar annealed films for two different thicknesses of 49 nm and 146 nm exhibiting similar RMS roughness values of about 13 nm in both the films. The roughness is much higher than those observed in Ar annealed films, and the nature of the roughness changes to more rounded features and apparently larger grains.

For comparison, surface morphology of the Ar and 7% H_2/Ar annealed films deposited on glass is shown in Fig. 2(a) and (b). The RMS roughness value is lower than those observed on PEN substrates. Further, Ar annealed films exhibited an RMS roughness value of 1.0 nm compared to 1.2 nm for the 7% H_2/Ar annealed films. The increased roughness value of 7% H_2/Ar annealed films compared with similar Ar annealed films is consistent with the results on PEN substrates and is summarized in Fig. 3.

3.2. Backscattering analysis

Fig. 4(a) and (b) depicts the 3.04 MeV oxygen resonance spectra of the Ar annealed ZnO:F thin films on a 200 μm PEN and glass substrate, respectively. The area of the O peak near channel 210 has been used to quantify the oxygen content of the ZnO:F films. The results from these as well as as-deposited films on glass and PEN substrates for 80 nm thick films are listed in Table 2. Though the data is limited, it is observed that O vacancies are slightly higher both for films deposited on PEN substrates and films that underwent Ar annealing. In contrast, the Zn/O ratio decreases after 7% H_2/Ar annealing. F was detected by

Table 1
RMS roughness values for given film thicknesses and annealing ambient for films on PEN and glass substrates. Grain size values are determined from AFM software, while the values inside the parentheses indicate grain size values determined from XRD using Eq. (1). The last column in this table displays the percentage of critical strain for various annealed samples at its respective critical radius.

Substrate	Annealing ambient	Film thickness (nm)	RMS roughness (nm)	Grain size (nm)	Critical strain (%)
PEN	As-deposited	146	9.7	15 (15)	–
PEN	Ar	49	1.4	16	1.005
PEN	Ar	94	3.0	17 (19)	0.767
PEN	Ar	226	7.8	22	0.613
PEN	7% H_2/Ar	49	13	22	1.005
PEN	7% H_2/Ar	146	13.5	24 (25)	–
glass	Ar	89	1.0	7.8	–
glass	7% H_2/Ar	89	1.2	12	–

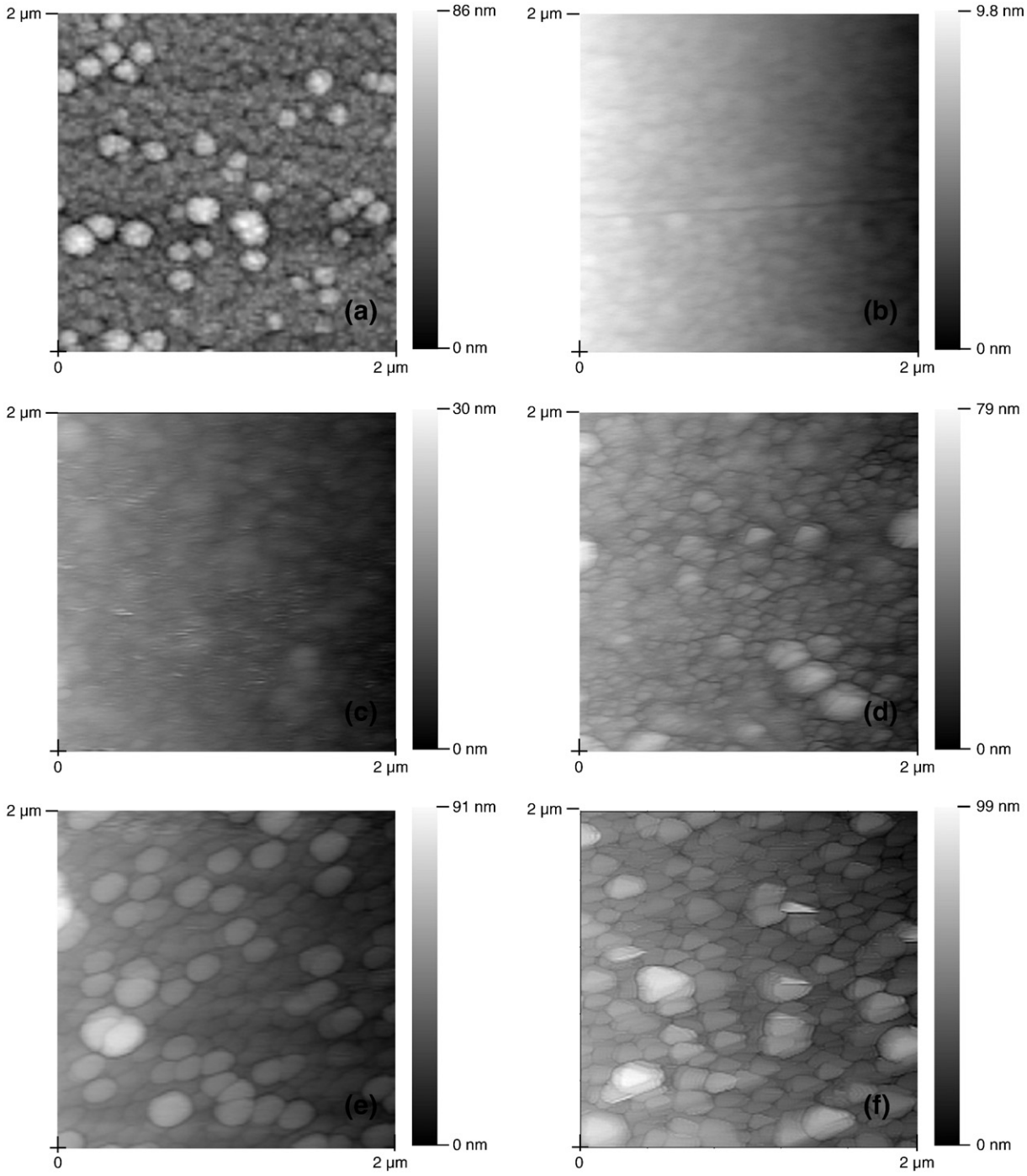

Fig. 1. 2 μm × 2 μm AFM images of ZnO:F films deposited on PEN substrates of thickness: (a) 146 nm, as-deposited; (b) 49 nm, Ar annealed; (c) 94 nm, Ar; (d) 226 nm, Ar; (e) 49 nm, 7% H_2/Ar, and (f) 146 nm, 7% H_2/Ar.

secondary ion mass spectroscopy (SIMS) analysis, and due to the lack of a standard, the exact composition could not be determined. However, F was not detected by RBS. Since the detection limit of F by RBS is about 0.25 at.%, this value represents the upper limit of F that can be present in the film.

3.3. XRD analysis

X-ray patterns were taken on numerous samples. No change in intensity or full width half maxima (FWHM) in the various X-ray peaks for PEN was observed between as-deposited and annealed films, indicating no significant change in substrate crystallinity during annealing. Fig. 5(a–c) illustrates X-ray patterns of an as-deposited film and annealed films on PEN substrates in Ar and 7% H_2/Ar ambients, respectively. The broad crystalline peaks corresponding to the PEN, and peaks corresponding to the preferred (002) orientation of ZnO were observed. The intensity of the (002) peak improves with annealing, with 7% H_2/Ar annealed films yielding the highest crystallinity. Absence of peaks from other major orientations does not preclude these, as PEN peaks are large and mask any weak peaks. The FWHM also decreased from 250 arc sec for the as-deposited film to 150 arc sec for the 7% H_2/Ar annealed film.

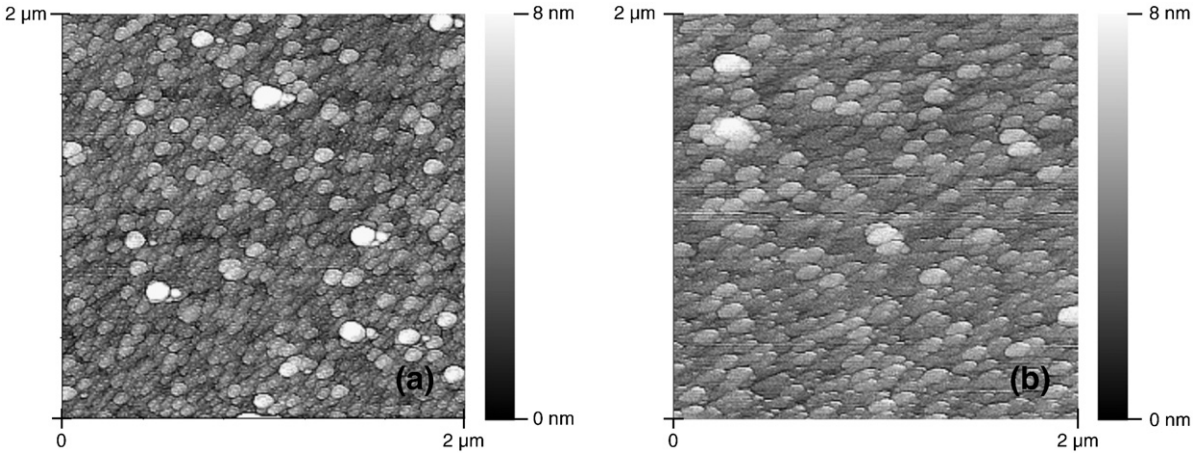

Fig. 2. 2 μm × 2 μm AFM images of ZnO:F films deposited on glass substrates of thickness: (a) 89 nm, Ar annealed and (b) 89 nm, 7% H_2/Ar annealed.

Furthermore, no dependence on the thickness of the films was observed.

3.4. Optical analysis

Fig. 6 exhibits the optical transmission between 350 nm and 800 nm of a bare PEN substrate for reference, as-deposited films, Ar annealed, and 7% H_2/Ar annealed films of four different thicknesses on PEN substrates. The average transmission T between 450 nm and 650 nm is in the range of 78 to 80% for thickness up to 150 nm regardless of annealing condition, as shown in Fig. 7(a). Fig. 7(b) shows the optical band gap as a function of thickness. For a higher thickness of 225 nm, T reduces significantly to 65%. The transmission of ZnO:F films on glass was found to vary from 70% to 87%. It is to be pointed out that transmission and reflection of bare PEN substrates annealed in Ar and 7% H_2/Ar ambients did not show any significant changes with respect to bare PEN substrates, which is consistent with what was reported by H. Han et al. [21]. Fig. 8 displays the corresponding absorption spectra determined from the respective transmission and reflection spectra. The optical gap was determined using band to band absorption given by $\alpha \propto (h\nu - E_g)^{1/2}$ [22], where E_g and $h\nu$ represent the band gap and incident photon energy, respectively. The optical gap was determined from the extrapolation of the linear part of the α^2 vs. $h\nu$ plot. The absorption edge of the films deposited on PEN substrates were approximately 3.2 eV, while films deposited on glass varied from 3.3 to 3.5 eV, which depended on film thickness.

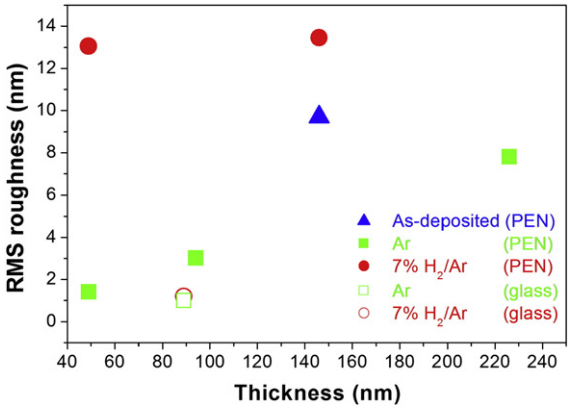

Fig. 3. Variation in surface roughness with film thickness for as-deposited and annealed films on glass and PEN substrates.

3.5. Electrical analysis

Fig. 9(a–c) illustrates the thickness dependence of the electrical transport parameters of the films annealed in Ar and 7% H_2/Ar ambients, deposited on the PEN substrates. No significant effect of the annealing ambient on the electrical parameters was observed for thicknesses beyond 75 nm. The carrier concentration increases with a corresponding decrease in mobility with thickness. For thinner 50 nm films, 7% H_2/Ar annealed films have a lower carrier concentration than Ar annealed films of the same thickness, while the mobility is higher. The resulting resistivity is independent of annealing ambient, is highest for thinner films, and is invariant for thicknesses beyond 75 nm. The mobility values of these films ranged from 3 to 11 cm^2/V-s. For reference, the resistivity variation with thickness deposited on the glass is displayed in Fig. 10. The resistivity is not significantly influenced by annealing or thickness and compares well with those values obtained on PEN for thicker films. The N and μ of films deposited on glass ranged from 2×10^{19}/cm^3 to 1.6×10^{20}/cm^3 and from 3 to 9 cm^2/V-s, respectively.

3.6. Bend testing

Fig. 11 illustrates typical variation of the resistance as a function of the radius of curvature, where tensile strain is generated by bending of the film. The critical radius for films was measured to be the intersection point of the gradual increase with the sharp rise in the resistance with decreasing radius. Fig. 12 exhibits the variation of the critical radius as a function of thickness for as-deposited and annealed films on a PEN substrate of 200 μm. It is to be noted that Fig. 11 displays only the data for selected films though data was collected on numerous samples, and these are plotted in Fig. 12. The R/R_0 ratio in Fig. 11 is a function of the collapsing radius, where R is the measured resistance and R_0 is the initial resistance. Both the critical radius values and the shape of the bending curve are strongly influenced by the thickness of the films and are insensitive to the annealing ambient. As thickness decreases, the critical radius decreases and the curves exhibit a steeper increase.

4. Discussion

Surface morphology of the films is found to be dependent on the thickness of the films as well as the annealing ambient. On both glass and PEN, thinner films annealed in an Ar ambient exhibit an RMS roughness value approximately equal to that of the substrate. The higher degree of roughness observed in thicker films and 7% H_2/Ar annealed films are due to the growth mechanism as per the following discussion. The grain size of the films measured from AFM is found to

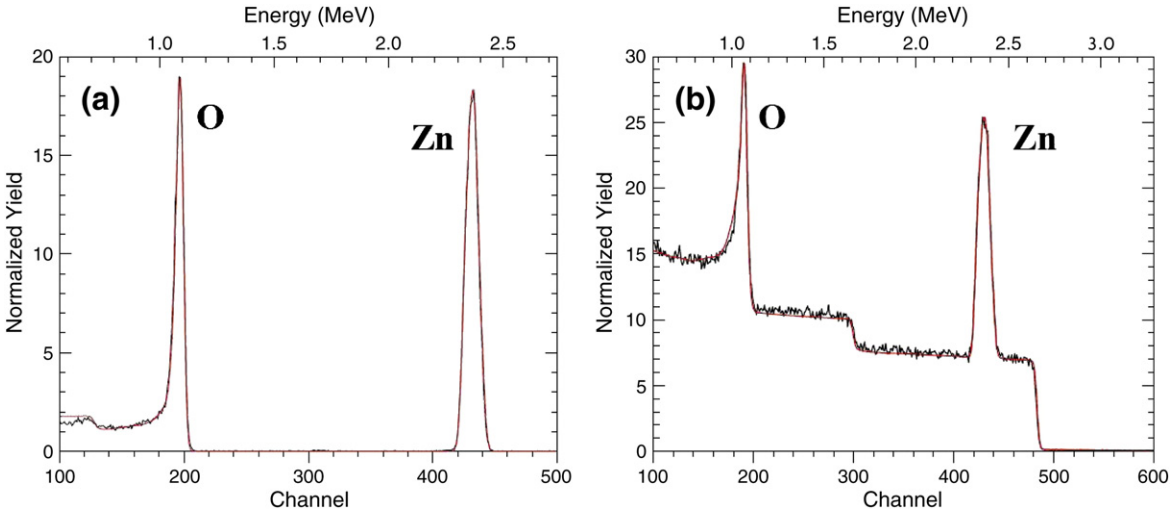

Fig. 4. RBS spectra of Ar annealed films on (a) PEN substrate and (b) glass substrate.

be in excellent agreement with those determined from the FHWM of the XRD data on selected samples, using Scherrer's equation [23]

$$D = \frac{0.9\lambda}{\beta \cos\theta} \quad (1)$$

where λ, β, and θ are the X-ray wavelength (0.15406 nm), FWHM, and Bragg diffraction angle, respectively, and the results are given in Table 1. Grain size increases on annealing, with 7% H_2/Ar annealed films exhibiting larger grain size and roughness than Ar annealed films. The data in Table 1 show excellent correlation between grain size and RMS roughness values. This suggests that (a) smaller grains coalesce with increasing film thickness, and (b) annealing in 7% H_2/Ar promotes grain growth. Changes in morphology for TCOs annealed in various inert vs. H_2 ambients have been demonstrated, but at higher temperatures than those used in this study [24]. Therefore, the mechanism for enhanced grain growth in the presence of H_2 cannot be determined from the current study. The RMS roughness value of the films deposited on PEN is almost one order of magnitude larger than those on glass, due to the differences in the initial roughness of the substrate itself.

The as-deposited as well as annealed films are found to be *c*-axis oriented exhibiting a preferred (002) orientation, consistent with the published reports [3,25–27] on ZnO films. Annealing improves the crystal quality, with 7% H_2/Ar annealing yielding better results than Ar annealing, consistent with higher grain size.

Variation in electrical parameters shows a stronger dependence on thickness than on the annealing ambient. The resistivity values decrease dramatically for films thicker than 70–80 nm on PEN substrates, while a smaller gradual decrease of resistivity with thickness is observed on the films deposited on glass. The resistivity values for thicker films of 200–250 nm are similar on PEN and glass substrates. This suggests that the first 50 nm deposited on PEN is highly defective, and can be attributed to the differences in surface energy values with the surface energy of PEN being lower than that of glass [28]. Ar annealed films on PEN substrate show a larger decrease in the carrier concentration as film thicknesses decreases below 100 nm, as compared to 7% H_2/Ar annealed films. Also, higher oxygen vacancies are observed on Ar annealed films, particularly on PEN substrates, as attested to by RBS data. Thus, Ar annealing appears to be more effective in altering the stoichiometry of the films. It is to be noted that the charge carriers in these films are produced by contributions from oxygen vacancies, F dopant incorporation either in the O lattice site or oxygen vacancies and interstitials of F and Zn. It is most likely that F occupies a fraction of the oxygen vacancy sites resulting in lower carrier concentration in thinner Ar annealed films, analogous to those reported by Yoon et al. [15] and Soliman et al. [29]. This explains the large variations observed in carrier concentration in these films.

Doping efficiency is defined [6] as the number of free electrons to that of F-doped atoms in a film, which was calculated to be 95% in our films. Assumed in the calculation, is that each F atom is incorporated only in the substitutional O site, yielding one free electron and a film with 0.25 at.%F concentration (the upper limit set by the RBS measurement, as earlier discussed). The presence of F was detected by SIMS in these films. Such low incorporation of F with respect to the target was also reported by Yoon et al. [15] on their films prepared by RF sputtering. It is to be noted that high carrier concentrations of

Table 2
Lists the Zn/O ratio determined from RBS on 80 nm thick as-deposited and annealed films.

Substrate	Zn/O ratio		
	As-deposited	Ar annealed	7% H_2/Ar annealed
Glass	1.00/1.00	1.08/1.00	–
PEN	1.07/1.00	1.10/1.00	1.02/1.00

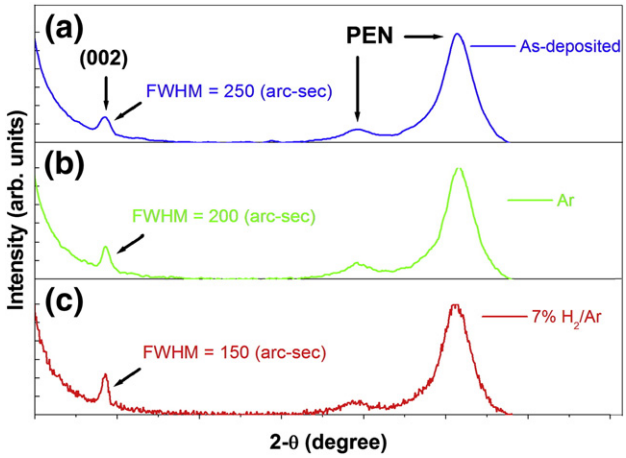

Fig. 5. X-ray patterns of (a) as-deposited films, (b) Ar annealed films and (c) 7% H_2/Ar annealed films on PEN substrates.

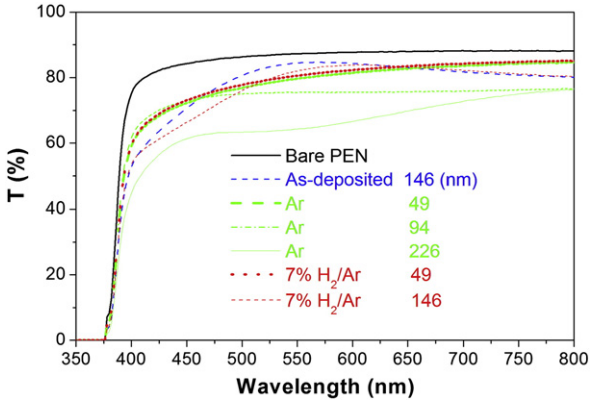

Fig. 6. Transmission spectra for various thicknesses of ZnO:F films on PEN substrates.

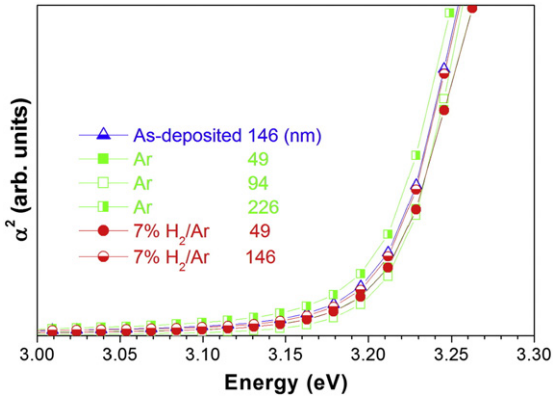

Fig. 8. Square of the absorption coefficient as a function of photon energy for ZnO:F films on PEN substrates.

$6.7\times10^{20}/\mathrm{cm}^3$ with 10^{-3} ohm-cm resistivity was obtained in the films deposited on glass, which were subjected to higher annealing temperatures of 200 °C in ultra high vacuum. This carrier concentration coincidently corresponds to about 1.7 at.% F doping in the film which is the same as the concentration in the target. Though this data appears to suggest 100% doping efficiency by F, doping by oxygen vacancy cannot be ruled out, as discussed below. Thus, incorporation and activation of F in the film appears to be dependent on the nature of the substrate and sensitive to the annealing temperature as well as the ambient.

Fig. 13 exhibits the dependence of mobility on carrier concentration for all of the annealed films both on PEN and glass. The different scattering mechanisms that may limit the mobility of carriers are ionized impurity, lattice and grain boundary scattering. Among these the contribution of grain boundary scattering can be neglected as the grain sizes ranged from 9 to 24 nm, which are much larger than the mean free path l of the carriers, computed to be ≈2 nm from the following equation: [6]

$$l = \left(\frac{h}{e}\right)\left(\frac{3N}{\pi}\right)^{\frac{1}{3}}\mu \tag{2}$$

where μ represents the mobility, e the electron charge, h *is* Planck's constant and N is the carrier concentration. Secondly, the grain boundary potential diminishes significantly for the carrier concentrations under study [30]. Finally, the mobility of thinner 7% H_2/Ar annealed films is found to be tenfold smaller than the corresponding Ar annealed films, while there is little corresponding change in grain size. These attest to a negligible contribution to mobility from grain boundary scattering. It has been reported [31] that mobility due to lattice scattering is relatively low, a typical value being 210 cm^2/V-s for ZnO films at room temperature and hence cannot be completely neglected. A good fit to the experimental data is shown in Fig. 13, and was obtained by taking into account the ionized impurity scattering expression μ_{ii} derived by Conwell, Weisskopf and Shockley [31–33] for a degenerate semiconductor, as given in the equation below

$$\mu_{ii} = \frac{3(\varepsilon_r\varepsilon_0)^2h^3}{Z^2m^{*2}e^3}\left\{\ln\left[1+\left(\frac{3^{2/3}\pi^{1/3}\varepsilon_r\varepsilon_0h^2N^{1/3}}{2m^*e^2}\right)^2\right]\right\}^{-1} \tag{3}$$

along with the lattice impurity scattering μ_{lat} (210 cm^2/V-s) using Matthiessen's rule

$$u = \frac{\mu_{lat}\mu_{ii}}{\mu_{lat}+\mu_{ii}} \tag{4}$$

where m^* is the effective mass, ε_r is the relative static permittivity, ε_0 is the permittivity of free space and Z is the charge state. In our case the best fit was obtained for $Z=2$ corresponding to doping by oxygen vacancies [31]. Thus scattering by oxygen vacancies appears to be the dominant scattering mechanism limiting the mobility of carriers.

Transmission of the films on PEN was as high as 80% and decreases significantly for thicknesses higher than 150 nm. The absorption edge is around 3.2 eV with a maximum shift of 10 meV with increasing carrier concentration. This value is lower than the absorption edge of ZnO due to the large absorption coefficient of PEN substrate in this range. The absorption edges of the films deposited on the glass are higher and in good agreement with the published results on doped

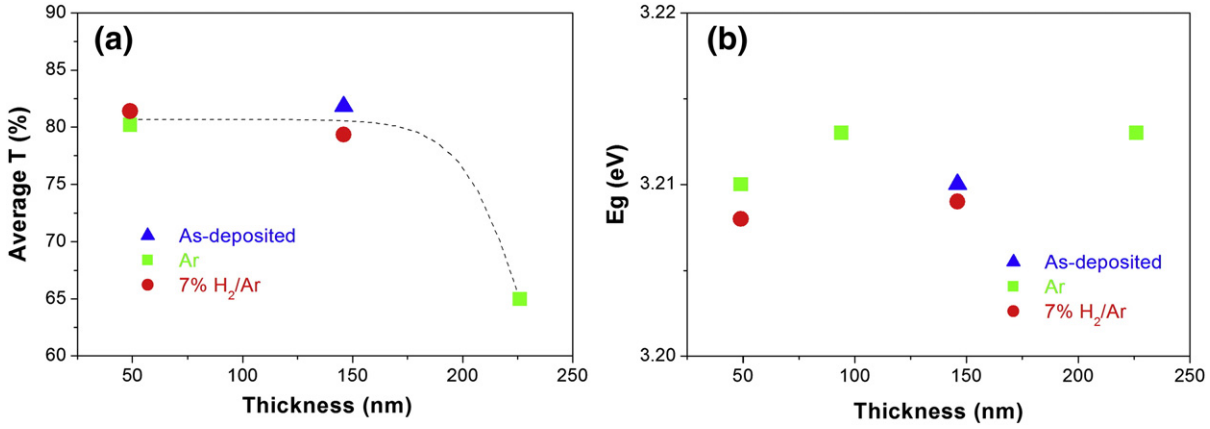

Fig. 7. (a) Variation of average transmission of the films in the 450–650 nm range with thickness on PEN and (b) optical band gap as a function of thickness on PEN substrates.

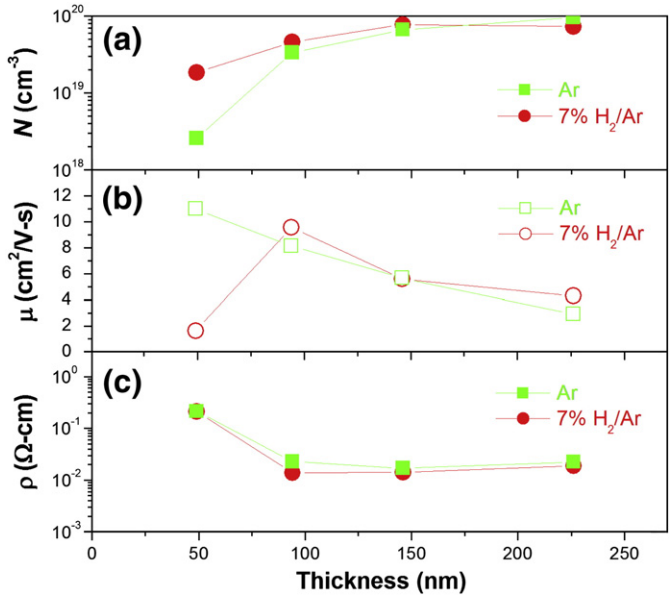

Fig. 9. (a) Carrier concentration, (b) mobility, and (c) resistivity as a function of film thickness deposited on PEN substrates.

ZnO films [34–36] for similar ranges of carrier concentration. The maximum observed shift in absorption edge of 150 meV is attributed to Burstein–Moss shift [37,38] due to the filling of the conduction band with increasing carrier concentration and is given by

$$\Delta E_g = \left(\frac{1}{1+\frac{m_e}{m_h}}\right) \times 2kT \times \ln\left(\frac{N}{\sqrt{N_c N_v}}\right) + 4kT \quad (5)$$

where N is the measured electron carrier concentration, N_c and N_v are the effective density of conduction and valence-band states, k is the Boltzmann's constant, and T is the temperature in degree Kelvin, respectively. ΔE_g represents the band gap shift at a given carrier concentration, m_e and m_h are the conduction and valence-band effective mass, respectively. With $m_e = 0.28\ m_0$ and Eg of ZnO as 3.3 eV, the band gap shift of 200 meV for a carrier concentration of 1.4×10^{20}/cm^3, calculated from the above model is found to be in good agreement with the experimental shift of 150 meV observed.

The critical radius of the films is considered as a failure criterion for bend testing [20]. When the substrate and film is bent, the top film surface experiences a tensile strain, while the bottom surface of the substrate is subjected to compressive strain. One plane between the two corresponds to no strain, referred to as a neutral surface. The distance from the top surface to this neutral plane is a measure of the strain on the top surface. As the Young's modulus of ZnO (121 GPa) [39] is much higher than that of the PEN substrate (5 GPa) [16], the neutral surface plane is shifted towards the top surface and hence reduces the strain of the films. The critical strain was computed using conventional beam theory [40], based on the observed critical radius varying from 6.5 to 17.0 mm. These are in the range of 1.0 to 0.6% and are tabulated in Table 2. These are consistent with the typical strains at which microcracks appear in oxide thin films deposited on flexible substrates [41].

The critical strain that can be accommodated by the film was found to be a function of thickness, where the strain is larger in thinner films, as tabulated in Table 1. The thickness dependence of critical strain and critical radius can be satisfactorily explained by Griffith defect theory [42]. The common cause for the fracture of the film and the loss of electrical conductivity in the films is attributed to the formation and propagation of microcracks through the film thickness and in plane. These microcracks may originate from pin holes in the films, embedded voids from deposition, and/or surface defects from the underlying PEN substrates. Several components could contribute to the lower critical strain in thicker films. For example, the coalescing of grains and reduction in defect density with increased film thickness, as observed by AFM and electrical measurements respectively, suggest higher compressive strain in the

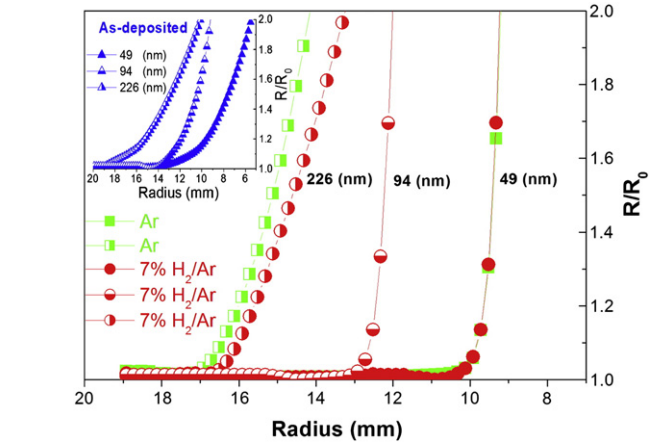

Fig. 11. Collapsing bend test results for as-deposited, Ar annealed and 7% H_2/Ar annealed films.

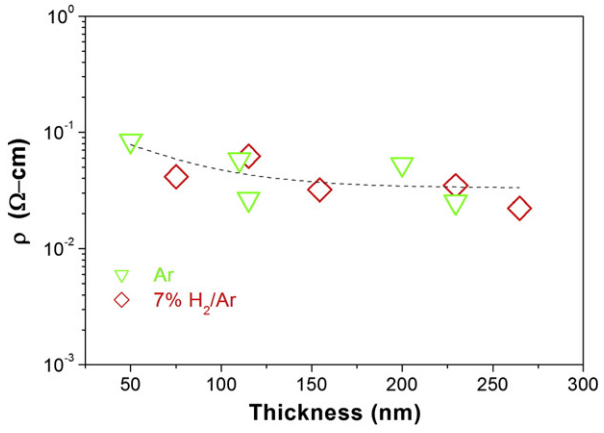

Fig. 10. Dependence of the resistivity on the film thickness deposited on glass substrates.

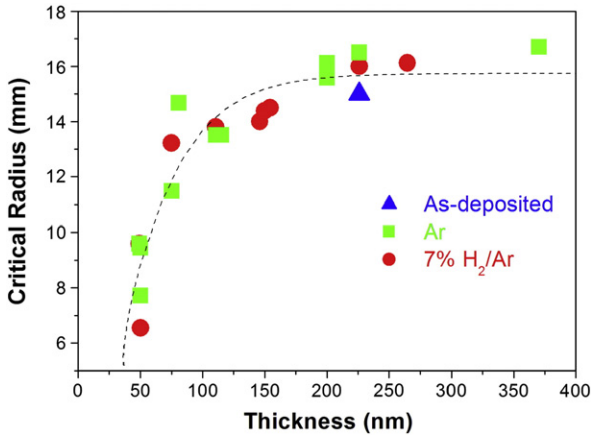

Fig. 12. Variation of critical radius with film thickness.

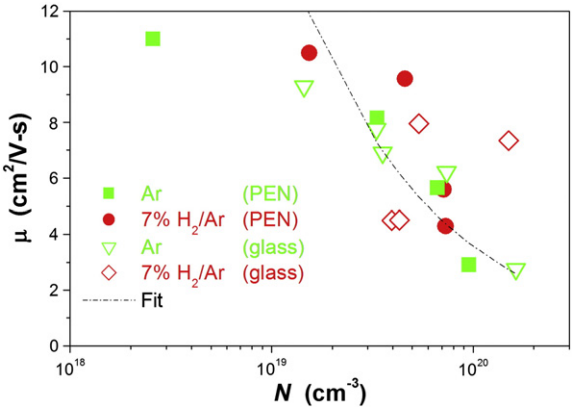

Fig. 13. Mobility variation as a function of carrier concentration on films deposited on glass and PEN substrates. Dashed line indicates the theoretical fit from Conwell, Weisskopf and Shockley equation with Z = 2.

thinner, defective films. Internal compressive stress would result in a higher bending strain required to reach the failure strain. Similar reasoning can be applied for the differences in the shape of the curve observed between the annealed films and the as-deposited films. In the annealed films, the grain sizes are larger, defects and residual stresses are less and hence there is less resistance to crack propagation. This is reflected in the steeper failure curve observed in these films. It is to be noted that the thermal stress that might arise due to a rise in temperature at the surface of the PEN substrate during deposition, (ΔT~20 °C) was estimated to be less than the internal stress in the film [43] and hence has been neglected.

5. Conclusion

The properties of ZnO:F films deposited by RF sputtering on PEN substrates have been correlated to the thickness of the films and annealing ambient. Annealing in 7% H_2/Ar resulted in substantial grain growth and increased surface roughness, but had a significant effect on optical or electrical properties only for films thinner than 100 nm. At a thickness of 100 nm the annealed films deposited on PEN substrate reveal high transmission of 80%, $N = 6.7\times10^{19}/cm^3$, $\mu = 9.5\ cm^2/V\text{-}s$ and $\rho = 1.3\times10^{-2}\ \Omega\text{-}cm$. The electrical transport properties were explained using the ionized impurity and lattice scattering mechanisms, and were identified as predominantly due to O vacancy scattering. The bending radius was used as a measure of the mechanical flexibility for films deposited on 200 μm thick PEN substrates. Both annealing and thickness of the films determine the critical strain beyond which the failure of the film occurs, which in turn influences the critical radius of bending.

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References

[1] S. Fay, U. Kroll, C. Bucher, E. Vallat-Sauvain, A. Shah, Sol. Energy Mater. Sol. Cells 86 (2005) 385.
[2] X. Yu, J. Ma, F. Ji, Y. Wang, X. Zhang, C. Cheng, H. Ma, J. Cryst. Growth 274 (2005) 474.
[3] K. Chen, K.S. Chiang, H.P. Chan, P.L. Chu, Opt. Mater. 30 (2008) 1244.
[4] E. Fortunato, A. Gonçalves, V. Assunção, A. Marques, H. Águas, L. Pereira, I. Ferreira, R. Martins, Thin Solid Films 442 (2003) 121.
[5] Y. Liu, Y. Zang, G. Wei, J. Li, X.L. Fan, C. Cheng, Mater. Lett. 63 (2009) 2597.
[6] Z.L. Pei, X.B. Zhang, G.P. Zhang, J. Gong, C. Sun, R.F. Huang, L.S. Wen, Thin Solid Films 497 (2006) 20.
[7] R.G. Gordon, MRS Bull. 25 (2000) 52.
[8] Y. Han, D. Kim, J.S. Cho, Y.W. Beag, S.K. Koh, V.S. Chernysh, J. Appl. Phys. 97 (2005) 024910.
[9] A. Maldonado, A. Guillén-Santiago, M. de la L. Olvera, R. Castanedo-Pérez, G. Torres-Delgado, Mater. Lett. 59 (2005) 1146.
[10] A. Maldonado, S. Tirado-Guerra, M. de la L. Olvera, J. Phys. Chem. Solids 70 (2009) 571.
[11] A. Maldonado, S. Tirado-Guerra, M. Meléndez-Lira, M. de la L. Olvera, Sol. Energy Mater. Sol. Cells 90 (2006) 742.
[12] A. Sanchez-Juarez, A. Tiburcio-Silver, A. Ortiz, E.P. Zironi, J. Rickards, Thin Solid Films 333 (1998) 196.
[13] S.S. Shinde, P.S. Shinde, S.M. Pawar, A.V. Moholkar, C.H. Bhosale, K.Y. Rajpure, Solid State Sci. 10 (2008) 1209.
[14] Y.Z. Tsai, N.F. Wang, C.L. Tsai, Mater. Lett. 63 (2009) 1621.
[15] H.S. Yoon, K.S. Lee, T.S. Lee, B. Cheong, D.K. Choi, D.H. Kim, W.M. Kim, Sol. Energy Mater. Sol. Cells 92 (2008) 1366.
[16] W.A. MacDonald, M.K. Looney, D. MacKerron, R. Eveson, R. Adam, K. Hashimoto, K. Rakos, J. Soc. Inf. Disp. 15 (2007) 1075.
[17] T.L. Alford, L.C. Feldman, J.W. Mayer, Fundamentals of Nanoscale Film Analysis, Springer, New York, 2007.
[18] S.W. Russell, A.E. Bair, T.L. Alford, T.E. Levine, Nucl. Instrum. Methods Phys. Res. Sect. B 118 (1996) 201.
[19] L.R. Doolittle, Nucl. Instrum. Methods Phys. Res. Sect. B 9 (1985) 344.
[20] S. Grego, J. Lewis, E. Vick, D. Temple, J. Soc. Inf. Disp. 13 (2005) 575.
[21] H. Han, J.W. Mayer, T.L. Alford, J. Appl. Phys. 100 (2006) 083715.
[22] K. Sivaramakrishnan, T.L. Alford, Appl. Phys. Lett. 94 (2009) 052104.
[23] L.V. Azaroff, Elements of X-ray Crystallography, McGraw-Hill, New York, 1968.
[24] Y.H. Yun, H.W. Han, M.J. Choi, S.C. Choi, J. Ceram. Process. Res. 6 (2005) 259.
[25] P. Sharma, K. Sreenivas, K.V. Rao, J. Appl. Phys. 93 (2003) 3963.
[26] T.M. Barnes, J. Leaf, C. Fry, C.A. Wolden, J. Cryst. Growth 274 (2005) 412.
[27] J.J. Lu, S.Y. Tsai, Y.M. Lu, T.C. Lin, K.J. Gan, Solid State Commun. 149 (2009) 2177.
[28] Steven Label, Substrate's Dynes/Cm[cited 2009 11/02]; Available from:, http://www.stevenlabel.com/Dyne.htm1998.
[29] M. Soliman, M.M. Hussein, S. El-Atawy, M. El-Gamal, Renew. Energ. 23 (2001) 463.
[30] J. Bruneaux, H. Cachet, M. Froment, A. Messad, Thin Solid Films 197 (1991) 129.
[31] K. Ellmer, J. Appl. Phys. 34 (2001) 3097.
[32] E. Conwell, V.F. Weisskopf, Phys. Rev. 77 (1950) 388.
[33] W. Shockley, Electrons and Holes in Semiconductors, D. Van Nostrand Company, Inc., Princeton, 1950.
[34] F. Quaranta, A. Valentini, F.R. Rizzi, G. Casamassima, J. Appl. Phys. 74 (1993) 244.
[35] K.C. Park, D.Y. Ma, K.H. Kim, Thin Solid Films 305 (1997) 201.
[36] K.H. Kim, K.C. Park, D.Y. Ma, J. Appl. Phys. 81 (1997) 7764.
[37] E. Burstein, Phys. Rev. 93 (1954) 632.
[38] R. Pino, Y. Ko, P.S. Dutta, S. Guha, L.P. Gonzalez, J. Appl. Phys. 96 (2004) 5349.
[39] T. Shibata, K. Unno, E. Makino, Y. Ito, S. Shimada, Sens. Actuators A Phys. 102 (2002) 106.
[40] S.P. Timoshenko, J.N. Goodier, Theory of Elasticity, McGraw-Hill, New York, 1970.
[41] S. Grego, J. Lewis, E. Vick, D. Temple, Thin Solid Films 515 (2007) 4745.
[42] A.A. Griffith, Proc. 1st Int. Congr. Appl. Mech, 1924, p. 55.
[43] H.W. Lee, S.P. Lau, Y.G. Wang, B.K. Tay, H.H. Hng, Thin Solid Films 458 (2004) 15.